Stability Enhancement of Bi-Directional Voltage Source Converters in Modern Power Systems

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Abstract

In future modern power systems, reliability and resilience could be an extreme challenge caused by the stability issues of the bidirectional power converters (BPCs). The non-linear dynamics of DC link voltage (DCLV) of BPCs in interaction with the existing linear control schemes may decrease the stability margin and cause operating-point-dependent instability issues. Existing approaches may solve this issue by reducing the DCLV control loop bandwidth, which considerably degrades the system performance. To tackle this issue, first, the root cause of the instability challenge is analytically investigated, and then, a non-linear stabilizer control scheme based on Lyapunov theorem is proposed. Considering the non-linear dynamic of the BPCs and the interaction between dynamics of DC link voltage and AC currents in the proposed stabilizer, it guarantees the stability of the converter in both directions of power flow and the full range of loading conditions. The performance of the proposed scheme is verified through simulation of the system under various operating conditions, considering uncertainties, disturbances, and short-circuit events, and comparing it with that of prevalent controllers.

1. INTRODUCTION

The global paradigm shift toward green electrification technologies is increasingly intensified. Renewable energies, e-mobility, electronic transmission systems, microgrid and smart grid technologies, and energy storage systems are forerunner technologies facilitating decarburization [1]. Power electronics plays an underlying role in energy conversion process. In this subject, bidirectional power converter (BPCs) will be the commonly used elements for inverting and rectifying the electrical energy [2, 3]. BPCs will be the common-connection point for different technologies of renewable energies, battery energy storage systems, electronic DC loads and drive systems, electric vehicle charger stations, HVDC and etc. Unlike their extensive controllability and power grid supporting functions, they pose stability challenges to the power system [4-6].

Different types of converters driven stability issues in modern power systems are discussed in two Technical Reports (TR) by IEEE Power and Energy Society (PES) in PES TR 66 and PES TR 77 [4, 5]. These issues may occur over a wide frequency range from a few Hz up to several hundreds of kHz driven by converter controls including inner current control, voltage control, Phase-locked Loop (PLL), DC-link voltage control (DCLV), active and reactive power control, harmonics, and etc. [4, 5, 7]. Although the stability of current, power and harmonics control loops, considering the time delay in the digital control implementation and interaction with PLL are well addressed in the existing literature, only a few works has studied the DCLV control stability, which is the main focus of this paper.

In the field of power converter operation, the inverter mode has been the dominant operating mode in the most of studies till today. However, the introduction of hybrid AC/DC systems, energy storage systems, back-to-back converters, active rectifier for motor derive systems will further highlight the importance of operating in both modes of inverting and rectifying. Although, a BPC has the potential capability to operate in both rectifier/inverter modes, preserving its stability is a challenging issue. The subject that has been addressed in [8-11], and it is shown that the BPC may encounter instability issues especially in the rectifier mode and high dynamic performance with the prevalent control schemes.

DCLV dynamics in BPC has complex non-linear components due to the instantaneous power of the output filter which makes its analysis difficult. Most of existing methods ignore this non-linearity to simplify the DCLV dynamic model [12-14], and correspondingly, the DCLV controller design procedure, which hereafter is called "prevalent DCLV controller". The prevalent controller preserves the BPC stability in inverter mode; however, it is questionable under the rectifier mode with high control loop bandwidth (BW) [8, 9]. To improve the stability of DCLV loop, [9] has suggested two remedies of: 1) proposing a nonlinear controller

for the nonlinear dynamic of the DCLV, and 2) using small-signal linearized model of DCLV, instead of its simplified model, and proposing a linear controller, hereafter called "modified DCLV controller". The first suggested scheme is complex and not addressed in literature except in [15], which used the exact nonlinear model of DCLV and stabilized the DCLV using the intrinsic parallel resistance of its DC link capacitor. However, the high value of this resistance and its low damping effect do not guarantee the stability in practical application. On the other hand, the modified DCLV controller design scheme, combined with predictive control, is adapted in [16-20]. Also, the linearized model of DCLV is variously used to explored the DCLV stability [21, 22].

Although using the modified controller simplifies the analysis and the control design procedure, it is not compatible with the exact nonlinear model of DCLV. Therefore, it is necessary to decrease the bandwidth of DCLV control loop (BW_{dc}) for ensuring a stable control system. This limits the functionality, response speed and disturbance rejection capability of the BPC and leads to necessity of the larger DC-link capacitance and larger converter size [23, 24]. Furthermore, using the modified controller may lead to high-frequency oscillation due to the interactions with the current control dynamic, which is analyzed in [8, 21] by an impedance-based dynamic model. The instability of BPCs under rectifier mode of operation is also illustrated in [8], and it also recommend that BW_{dc} should be decreased from the inverter mode to the rectifier.

As a summary, there is still a gap on control design of BPCs, which could work for both inverter/rectifier modes of operation under different loading conditions with high enough bandwidth and suitable transient response. The subject that is complicated considering the nonlinear model of DCLV and its interaction with current control loop. Whereas, based on the best knowledge of authors, no definite control scheme has been presented considering exact nonlinear model of DCLV to meet the mentioned requirement.

In this regard, in this paper, first, both the nonlinear and small signal dynamic models of DCLV are analyzed in detail, and the root cause of the instability under rectifier mode of operation is investigated. Accordingly, a non-linear Lyapunov-based controller is proposed for DCLV control, which considers the nonlinear dynamic characteristics of DCLV and its interaction with output current dynamics. Using the proposed scheme, the system is stable with proper stability margin and tracking performance under all modes/operating conditions and under the presence of uncertainty in the parameters. The novelties and contribution of the paper are summarized as follows.

- Analyzing the non-linear dynamic model of DCLV and introducing the root cause of instability issue in DCLV with prevalent and modified controllers; and
- Proposing a non-linear Lyapunov-based DCLV controller considering the exact nonlinear model of DCLV and its interaction with the current control loop.

The remainder of this paper is organized as follows. Modeling and prevalent DCLV and current controls of a BPC are explained in Section II. Performance of prevalent DCLV control design scheme is analyzed in section III, and root cause of the instability issue of DCLV is illustrated. The proposed non-linear DCLV control scheme is presented in Section IV. The numerical analysis and the conclusion of the paper are given in sections V and VI, respectively.

2. MODELIING AND PREVALENT CONTROL OF BIDIRECTIONAL POWER CONVERTER

A general schematic diagram of a power converter with a generation (a PV array), battery storage and DC loads in the DC link is shown in Fig. 1. In the AC side, the converter is connected via output filters to the grid modeled by its Thevenin equivalent. Depending on the power generation/consumption status, the converter operates either in inverter or rectifier modes. When the PV power generation exceeds the power absorbed by loads and battery storage, the converter switches to inverter mode of operation. On the other hand, under the deficiency of power from the PV and storage to supply the load, the converter switches to rectifier mode. Thus, a stable operation of converter in both modes of operation is necessary to guarantee the continuous operation in both modes. In the following, the prevalent control structure of the converter is presented.

2.1 Modeling of Power Converter

The dynamic model of a power converter includes the dynamics of ac side filter and DC-link capacitor, which are given in (1)-(2), respectively.

$$L\frac{di_{abc}}{dt} = Ri_{abc} + v_{tabc} - v_{gabc} \tag{1}$$

$$\frac{1}{2}C_{dc}\frac{d}{dt}(V_{dc}^2) = P_{dc-2} - P_{dc-1} \tag{2}$$

In (1)-(2), L is the filter inductance, R models the resistance of the filter and the switching power loss, C_{dc} is the DC-link capacitor, i_{abc} and $v_{t,abc}$ are the terminal currents and voltages of the converter, $v_{g,abc}$ is the grid voltage at PCC, and V_{dc} is the DC-Link voltage. Moreover, P_{dc-2}, P_{dc-1}, and P_{ac} are the exchanged DC and AC powers shown in Fig. 1. The operator d/dt($\cdot$) denotes the differential operator.
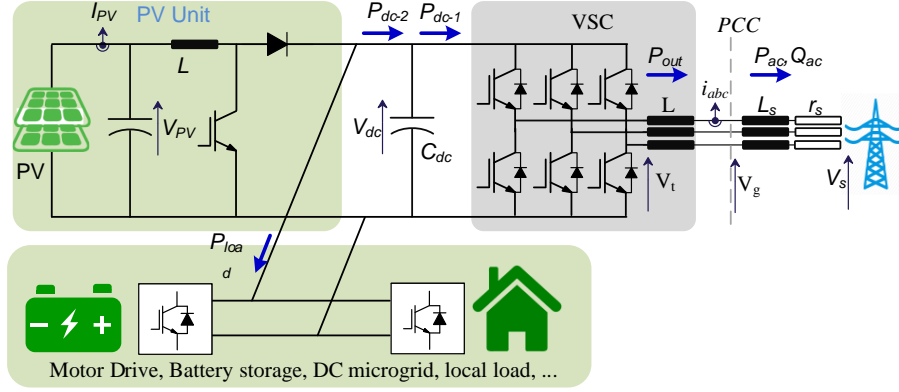
Fig. 1. Single line diagram of a bidirectional power converter.

By taking V_{dc} as a state-variable, (2) is non-linear; and to remove this nonlinearity, DC-link capacitor energy of $W_c = 0.5C_{dc}(V_{dc})^2$ is considered as a variable instead of V_{dc} [12]. Therefore, (2) can be rewritten as:

$$\frac{dW_c}{dt} = P_{dc-2} - P_{dc-1} \tag{3}$$

Transforming to the "dq" rotating reference frame, (1)-(2) are changed to (4)-(6).

$$\frac{di_d}{dt} = -\frac{R}{L}i_d - \omega \cdot i_q + \frac{(v_{td} - v_{gd})}{L} \tag{4}$$

$$\frac{di_q}{dt} = -\frac{R}{L}i_q + \omega \cdot i_d + \frac{(v_{tq} - v_{gq})}{L} \tag{5}$$

$$\frac{dW_c}{dt} = P_{dc-2} - P_{dc-1} \tag{6}$$

, where i_q, i_d and W_c are state variables, v_{td} and v_{tq} are control variables, and v_{gd} with v_{gq} are PCC voltages in "dq" reference frame, and ω denotes the grid angular frequency. Equation (7) represents the exchanged active power at PCC in Fig. 1, which can be simplified to (8) knowing that the value of v_{gq} is zeroed by the phase-locked-loop (PLL) operation.

$$P_{ac} = 1.5(v_{gd}i_d + v_{gq}i_q) \tag{7}$$

$$P_{ac} = 1.5(v_{gd}i_d) \tag{8}$$

The reactive power exchanged with AC grid is also given as:

$$Q_{ac} = 1.5(v_{gd}i_q) \tag{9}$$

Also, the instantaneous power of the output L filter will be obtained by differentiating its stored energy as

$$P_{L-inst} = \frac{3}{4}L\frac{d}{dt}(i_d^2 + i_q^2) \tag{10}$$

The net power loss of switching and filter resistance is:

$$P_{Loss} = \frac{3}{2}R(i_d^2 + i_q^2) \tag{11}$$

Now, by adding P_{L-inst} and P_{Loss} to P_{ac} of (8), P_{dc-1} is as

$$P_{dc-1} = \frac{3}{2}v_{gd}i_d + P_{L-inst} + P_{loss} \tag{12}$$

Substituting (12) in (6) yields (13), which shows the nonlinearity in the DC-link dynamics due to P_{L-inst}.

$$\frac{dW_c}{dt} = P_{dc-2} - \frac{3}{2}v_{gd}i_d - P_{L-inst} - P_{Loss} \tag{13}$$
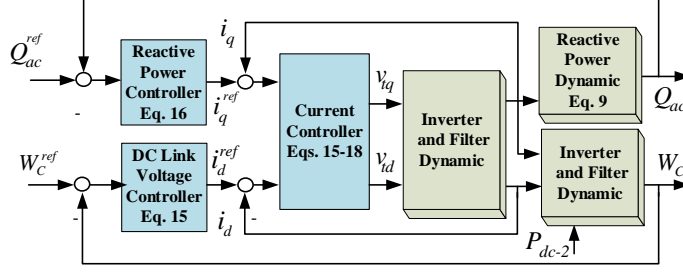
Fig. 2. Structure of prevalent DCLV control loop in power converter.

In the prevalent control scheme, P_{L-inst} and P_{Loss} are neglected in the DCLV model as given by (14) with this reasoning that both have small values compared to other terms. Also, P_{L-inst} has zero steady state value.

$$\frac{dW_c}{dt} \approx P_{dc-2} - \frac{3}{2}v_{gd}i_d \tag{14}$$

The P_{Loss} has positive damping effect on the stability of the control system, and it could be ignored for considering the worse possible condition in the controller design. However, ignoring P_{L-inst} may either reduce the stability margin or cause instability of the control system.

2.2 Prevalent Control of Power Converter

The prevalent control structure of a power converter can be stablished based on the equations of (4)-(5), (9), and (14). According to (9) and (14), the reactive power and DCLV are proportional to i_q and i_d, respectively. Thus, the reactive power and DCLV can be controlled by i_q and i_d with the references given in (15)-(16), respectively.

$$i_d^{ref} = {P_{dc-2}}\big/{1.5v_{gd}} + \frac{K_{p-w}s + K_{I-w}}{s}\left(W_c^{ref} - W_c\right) \tag{15}$$

$$i_q^{ref} = {Q_{ac}^{ref}}\big/{1.5v_{gd}} + \frac{K_{p-q}s + K_{I-q}}{s}\left(Q_{ac}^{ref} - Q_{ac}\right) \tag{16}$$

To control currents i_q and i_d, the control variables v_{td} and v_{tq} are determined as:

$$v_{td} = L \times K\frac{s + R/L}{s}(i_d^{ref} - i_d) + v_{gd} + L\omega i_q \tag{17}$$

$$v_{tq} = L \times K\frac{s + R/L}{s}(i_q^{ref} - i_q) + v_{gq} - L\omega i_d \tag{18}$$

Substituting (17) and (18) into (4)-(5), the dynamic behavior of i_d and i_q are as given by (19)-(20), in which K is the current control loop BW (BW_c).

$$i_d = \frac{K}{s+K}i_d^{ref} \tag{19}$$

$$i_q = \frac{K}{s+K}i_q^{ref} \tag{20}$$

The BW is limited by the computation and PWM time delays $T_d = 0.5/f_{sw}$, which are dependent on switching frequency (f_{sw}) [25]. As a rule of thumb, K is selected $0.1 \times f_{sw}$ to ensure an appropriate phase margin in the current control loop.

Prevalent control structure of power converter including DCLV (Eq. (15)), reactive power (Eq. (16)), curent control loops (Eq. (17)-(18)) is depicted in Fig. 2. As a rule of thumb, the bandwidth of the outer DC-link and reactive power control loops should be at least about 5 times lower than that of the inner current control loop BW_c, in the prevalent design scheme. Then, the outer control loops are designed independent from inner control loops.

3. PERFORMANCE EVALUATION OF REVALENT DCLV CONTROLLER

In this sub-section, the stability margin of the system with prevalent DCLV controller of (15)-(18) is investigated via analytical expressions and frequency domain study. It is shown that P_{L-inst} should not be ignored in DCLV controller design process, unlike it is done in the prevalent control, otherwise it may lead to undesirable dynamic response or even instability in DCLV control loop.

3.1 *Analytical Expressions*

Substituting (12) into (13) and ignoring P_{loss} as a pessimistic approximation, the result is given in (21).

$$\frac{dW_c}{dt} = P_{dc-2} - \frac{3}{2}v_{gd}i_d - \frac{3}{4}L\frac{d}{dt}(i_d^2 + i_q^2) \tag{21}$$

From (21), the dynamic equation of DCLV is nonlinear; and then, it is linearized around the operating point of (22)-(23) to use the linear systems stability analysis methods. Also, it is assumed that $W_c^0 = W_C^{ref}$ is DCL energy at operating point.

$$i_d^o = {P_{dc-2}}\Big/{1.5v_{gd}} \tag{22}$$

$$i_q^o = {Q_{ac}^{ref}}\Big/{1.5v_{gd}} \tag{23}$$

Substituting $i_d = i_d^0 + \Delta i_d$, $i_q = i_q^0 + \Delta i_q$, and $W_c = W_c^0 + \Delta W_c$ into (21), the resultant is:

$$\frac{d}{dt}(\Delta W_c) = P_{dc-2} - \frac{3}{2}v_{gd}(i_d^0 + \Delta i_d) - \frac{3}{4}L\frac{d(i_d^0 + \Delta i_d)^2}{dt} - \frac{3}{4}L\frac{d(i_q^0 + \Delta i_q)}{dt} \tag{24}$$

Considering (22), it is simplified to

$$\frac{d}{dt}(\Delta W_c) = -\frac{3}{2}v_{gd}\Delta i_d - \frac{3}{4}L\frac{d(i_d^{0^2} + 2i_d^0\Delta i_d + (\Delta i_d)^2)}{dt} - \frac{3}{4}L\frac{d(i_q^{0^2} + 2i_q^0\Delta i_q + (\Delta i_q)^2)}{dt} \tag{25}$$

Applying the first-order Taylor approximation to $(\Delta i_d)^2$ and $(\Delta i_q)^2$, and considering the zero value of $d(i_d^{0^2})/dt$ and $d(i_q^{0^2})/dt$, the small signal model of DCLV is as given in (26).

$$\frac{d}{dt}(\Delta W_c) = -\frac{3}{2}v_{gd}\Delta i_d - \frac{3}{2}Li_d^0\frac{d(\Delta i_d)}{dt} - \frac{3}{2}i_q^0L\frac{d(\Delta i_q)}{dt} \tag{26}$$

The Laplace representation form of (26) is given in (27).

$$\Delta W_c(s) = -\frac{3}{2}\frac{v_{gd} + Li_d^0 s}{s}\Delta i_d(s) - \frac{3}{2}Li_q^0\Delta i_q(s) \tag{27}$$

Whereas substituting $i_d = i_d^0 + \Delta i_d$ in (14) and taking Laplacian transform yields to the following simplified dynamic equation for DCLV.

$$\Delta W_c(s) = -\frac{3}{2}v_{gd}\frac{\Delta i_d(s)}{s} \tag{28}$$

Comparing (27) and (28) reveals that ignoring P_{L-inst} eliminates two terms in DCLV dynamic, which are (*i*) the $\Delta i_q(s)$ part in the right side of (27), and (*ii*) a "zero" at $s = v_{gd}/Li_d^0$. Therefore, the prevalent DCLV controller, which is designed based on (14), is by not considering the dynamics originated from such terms in the DCLV dynamic.

The $\Delta i_q(s)$ part in (27) shows the effect of the reactive current i_q on DCLV dynamic. According to (9) and (16), the reactive power dynamic is independent from i_d and W_c, and it does not affect DCLV stability. Hence, it can be regarded as a disturbance input for DCLV dynamic. On the other hand, the zero of $s = v_{gd}/Li_d^0$ is dependent on the operating point of the system (P_{dc-2}), which significantly affects the stability and dynamic characteristics of DCLV.

3.2 *Frequency Analysis*

Using the small-signal DCLV model of (27), prevalent DCLV controller in (15), and d-axis current dynamic in (19), the open loop small-signal transfer function of DCLV control loop is as given in (29). It is worth to mention that the disturbance part, i.e., $\Delta i_q(s)$, in (27) is ignored when calculating (29).

$$\Delta W_c(s) = \frac{-3}{2} \frac{v_{gd} + Li_d^0 s}{s} \frac{K}{s+K} \frac{K_{p-w}s + K_{I-w}}{s} \left(W_c^{ref} - W_c\right) \tag{29}$$

To get better insight about (29), the values taken by i_d^0 should be investigated. According to (22), during the inverter mode of operation, P_{dc-2} and consequently i_d^0 are positive. Then, the "zero" of $s = -\frac{v_{gd}}{Li_d^0}$ in (29) is located at the left-hand side of the S-plane. However, in rectifier mode of operation, P_{dc-2} is negative and the "zero" moves to the right half side of S-plane. Then, the DCLV becomes a non-minimum phase system in the rectifier mode of operation. This non-minimum phase "zero" reduces the phase margin, and may cause the instability of DCLV control loop as appears in the prevalent control of DCLV.

To further explain the performance of prevalent DCLV control and the impact of zero of $s = -\frac{v_{gd}}{Li_d^0}$, a frequency analysis is presented in the following. Assume a test power converter with the parameters given in Table I. The DCLV controller is given by (30),

$$i_d^{ref} = \frac{P_{dc-2}}{\frac{3}{2}v_{gd}} + \frac{360s + 40000}{s} \frac{1}{1.5v_{gd}} \left(W_c^{ref} - W_c\right) \tag{30}$$

where, $K_{p-w} = 360/1.5v_{gd}$ and $K_{I-w} = 4000/1.5v_{gd}$ are selected by prevalent control design scheme to get PM = 60 and BW_{dc}=340 rad/s. However, the frequency domain analysis based on linearized DCLV model of (27) shows that PM and GM will be non-constant and dependent to operating point. To more explain, the open loop frequency response of DCLV in (29) with the prevalent DCLV controller of (30) is shown in Fig. 3 for different values of P_{dc-2}, in which the frequency response is depicted with and without considering the zero of (29). Also, the vertical solid line in Fig. 3 shows the desired BW_{dc} (in this case 340 rad/s) for prevalent controller scheme. The following pointes are inferred from Fig. 3:

• Under inverter mode of operation ($P_{dc-2} > 0$), the "zero" is at the right-half side of s-plain, which adds positive phase to the system and increases the stability margin of DCLV.

• Under rectifier mode of operation ($P_{dc-2} < 0$), the "zero" is at left-half side of s-plain, which adds negative phases to the system and adversely affects the stability margin of the DCLV control loop. The more negative is P_{dc-2}, the more decreases the PM and stability.

• With increasing BW_{dc}, the solid line in the figure shifts to the right and the negative phase imposed by the zero becomes greater and the stability of the system is degraded more.
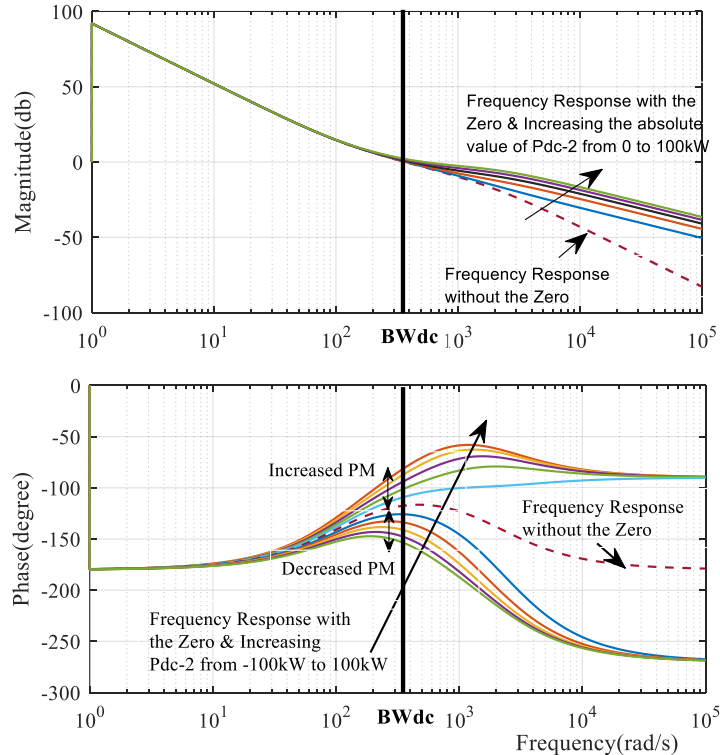

Fig. 3. Frequency response of the open loop system with and without the zero.

To sum up the above analyses, the PM of the closed-loop system is shown in Fig. 4 for different values of P_{dc-2}. It can be seen that in contrary to the expected constant PM = 60 in the prevalent controller scheme, the actual PM of the system decreases by increasing the P_{dc-2} toward more negative values; i.e., $P_{dc-2} = -100kW$, $PM = 15^o$. It will be shown that, the stability situation is far more serious with the actual nonlinear system such that the system becomes unstable for $P_{dc-2} < -80kW$.

TABLE I. Parameters of the sample power converter

Variables/Parameter	Symbol	Value
Nominal power	P_{nom}	100 kW
Line to line voltage	V_{LL}	380 V
Switching frequency	f_{sw}	4 kHz
DCLV	V_{dc}	1000 V
Filer inductor	L	3 mH
DC-link capacitor	C_{dc}	4 mF
Grid inductance	Ls	460 µH
Current control BW	BW_c/ K	2000 rad/s

In summary, to guarantee the stability of the system while using the prevalent controller, either BW_{dc} should be sufficiently decreased or P_{dc-2} should be limited in rectifier operating mode. Then, a compromise between "speed/power transfer capability of power converter" and "the stability margin of the DCLV" is required. To improve the stability and power transfer capability, the two following procedures can be considered.
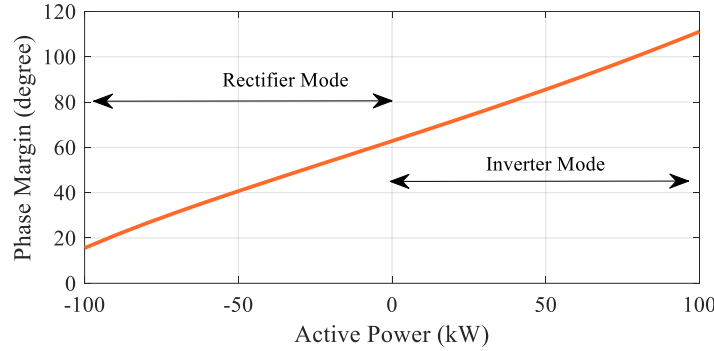

Fig. 4. Stability margin of DCLV dependent on operating point, in the case of using DCLV controller in (30), designed by the prevalent scheme.

1- Designing DCLV controller based on small-signal model of (27) instead of the simplified model of (14), which is named before "*modified controller*" [16-20]. As the model (27) is dependent on the operating point ($i_{d0} \propto P_{dc-2}$), the controller should be either adaptive or designed for the worst-case of operating point. Due to the complexity and unreliability of the adaptive controller, the controller design at worst-case operating point is preferred. The rectifier mode with maximum nominal power is selected for the design, which is associated with the most negative value of P_{dc-2}. Even with this remedy, BW_{dc} should be still reduced to preserve the stability, which is not a suitable characteristic.

2- Designing a nonlinear controller based on nonlinear dynamic model of (13), which is the most preferable/reliable but complex scheme. In this regard, a novel nonlinear controller is proposed in this paper to stabilize the DCLV system, which properly work regardless of the system operating point and with high values of BW_{dc}.

4. PROPOSED NIN-LINEAR DCLV CONTROLLER

The proposed non-linear DCLV control of this section guarantees a stable operation of the converter in both rectifier and inverter modes of operation with high BW_{dc}. The details are provided in the following.

In contrary to the prevalent controller, in the proposed controller, the output current and DCLV controllers are designed simultaneously, whereby their interaction is inherently considered in the design procedure. At the beginning, three error variables of e_1, e_2, and e_3 are defined as given by (31)-(33).

$$i_d = i_d^o + e_1 \tag{31}$$

$$i_q = i_q^o + e_2 \tag{32}$$

$$W_c = W_c^{ref} + e_3 \tag{33}$$

Also v_{td} and v_{tq} are defined as

$$v_{td} = Ri_d + L\omega.\,i_q + v_{gd} + u_d \tag{34}$$

$$v_{tq} = Ri_q - L\omega.\,i_d + v_{gq} + u_q \tag{35}$$

Substituting (31)-(35) into (4), (5), and (21) yields to (36)-(37).

$$\frac{de_1}{dt} = u_d \tag{36}$$

$$\frac{de_2}{dt} = u_q$$

$$\frac{de_3}{dt} = -1.5V_{gd}e_1 - 1.5Li_d^0\left(\frac{de_1}{dt}\right) - 1.5Le_1\left(\frac{de_1}{dt}\right) - 1.5Li_q^0\left(\frac{de_2}{dt}\right) - 1.5Le_2\left(\frac{de_2}{dt}\right) \tag{37}$$

Now, a new variable ρ is defined as follows.

$$\rho = e_1\beta_1 + e_2\beta_2 + e_3 \tag{38}$$

where,

$$\beta_1 = 1.5Li_d^0 + \frac{3L}{4}e_1 \tag{39}$$

$$\beta_2 = 1.5Li_q^0 + \frac{3L}{4}e_2 \tag{40}$$

Substituting (39)-(40) into (38), and with mathematical simplification, the dynamic equation of ρ is

$$\frac{d\rho}{dt} = -1.5V_{gd}e_1 \tag{41}$$

Also, the positive definite Lyapunov function can be defined by (42) to determine the control variables.

$$P = \frac{1}{2}\delta_1\rho^2 + \frac{1}{2}\delta_2e_1^2 + \frac{1}{2}\delta_3e_2^2 \tag{42}$$

Using Lyapunov function of (42), deriving all error variables to zero is questionable in the presents of uncertainty in the system. Hence, to guarantee a zero steady state error in control of reactive power and DC-link capacitor voltage, new variables F and H are defined as in (43) and added to dynamic equation of (36) and (41). This updated controller is robust against uncertainties in the system parameters and the delays originated from the PWM switching strategy and computations process.

$$\frac{dF}{dt} = \rho, \quad \frac{dH}{dt} = e_2 \tag{43}$$

By analyzing (38) along with (43), the variables ρ, e_3 and e_2 automatically driven to zero if F and H are properly stabilized to a steady state value; not necessarily to zero. Using the Lyapunov criterion, the following Lyapunov function is proposed in this paper, which provides suitable stability for the system.

$$V = \frac{1}{2}H^2 + \frac{1}{2}Z_h^2 + \frac{1}{2}F^2 + \frac{1}{2}Z_{f1}^2 + \frac{1}{2}Z_{f2}^2 \tag{44}$$

where,

$$Z_h = e_2 + k_{h1}H \tag{45}$$

$$Z_{f1} = \rho + k_{f1}F \tag{46}$$

$$Z_{f2} = -1.5v_{gd}e_1 + \left(k_{f1} + k_{f2}\right)Z_{f1} + \left(1 - k_{f1}^2\right)F \tag{47}$$

Then, the derivative of (44) with respect to the time is given in (48).

$$\frac{dV}{dt} = He_2 + Z_h(u_q + k_h e_2) + F\rho + Z_{f1}\frac{dZ_{f1}}{dt} + Z_{f2}[-1.5v_{gd}u_d + (k_{f1} + k_{f2})Z_{f1} + (1 - k_{f1}^2)F] \tag{48}$$

By simultaneous adding or subtracting $k_{h1}H^2$, $k_{f1}F^2$, and $k_{f2}Z_{f1}^2$ to the right side of (48), Eq. (49) is obtained.

$$\frac{dV}{dt} = -k_{h1}H^2 - k_{f1}F^2 + HZ_h + Z_h(u_q + k_h e_2) - k_{f1}F^2 - k_{f2}Z_{f1}^2 + Z_{f1}Z_{f2}\ Z_{f2}[-1.5v_{gd}u_d + (k_{f1} + k_{f2})Z_{f1} \\ + (1 - k_{f1}^2)F] \tag{49}$$

By selecting u_q and u_d according to (50) and (51), respectively, Eq. (49) is rewritten as shown in (52).

$$u_q = -(k_{h1}e_2 + H) - k_{h2}(e_2 + k_h H) \tag{50}$$

$$u_d = -\frac{1}{v_{gd}}[-Z_{f1} - (k_{f1} + k_{f2})Z_{f1} - (1 - k_{f1}^2)F - k_{f3}Z_{f2}^2] \tag{51}$$

$$\frac{dV}{dt} = -k_{h1}H^2 - k_{h2}Z_h^2 - k_{f1}F^2 - k_{f2}Z_{f1}^2 - k_{f3}Z_{f2}^2 \tag{52}$$

From (52), it is concluded that by (50) and (51), $\frac{dV}{dt}$ is definitely negative, and consequently, all variables of H, F, Z_h, Z_{f1}, and Z_{f2} go asymptotically to their steady-state values. According to (43) and its description, ρ and e_2 are derived to zero as the state variables F and H settle at their steady-state values. Also, according to Krasovskii-Lasalle principle [26], deriving ρ and e_2 to zero results in deriving e_3 to zero. Then, the control goal of deriving V_{dc} and Q_{ac} to their reference values is achieved. In summary, using the proposed nonlinear control scheme, the control goals are achieved, and stability of system is preserved regardless of the sign and value of P_{dc-2} . Furthermore, tracking speed and BW of system is adjustable by choosing proper positive values for k_{h1}, k_{h2}, k_{f1}, k_{f2}, and k_{f3} without any concern about instability in rectifier and inverter modes of operation. Indeed, using the proposed control scheme, operating modes and bandwidth of DCLV control don't threaten the bidirectional power converter stability.

Finally, the block diagram of the proposed controller is depicted in Fig. 5, in which different parts with refer to the associated equations are shown.
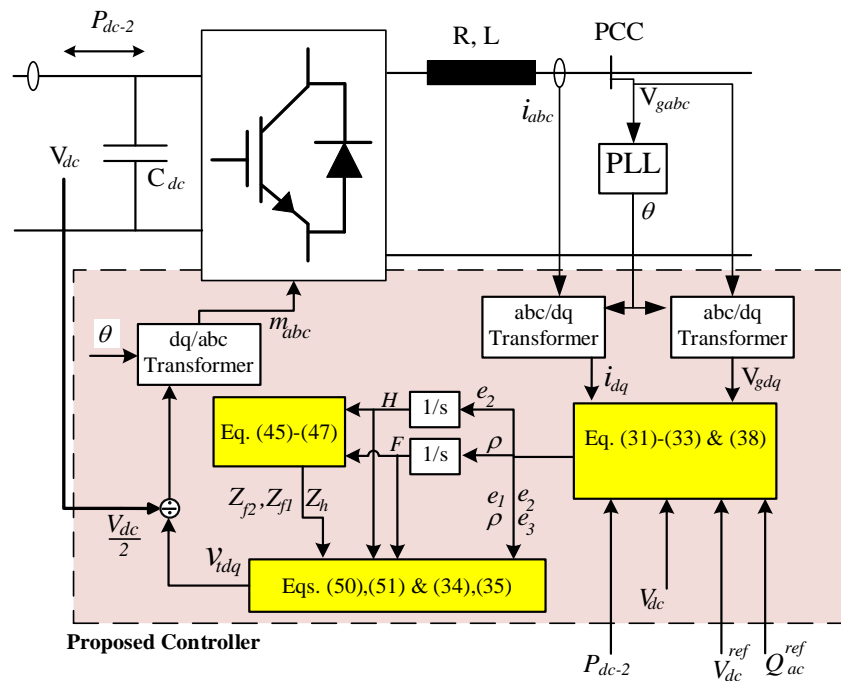

Fig. 5. Block diagram of proposed nonlinear DCLV control scheme.

5. SIMULATION RESULTS

To verify the effectiveness of the proposed control scheme, a comprehensive set of simulations have been done on the test converter with the parameters given in Table I. Also, the following assumptions are included, which accurately considers the real-life limitations.

a- The computational delay of $0.5/f_{sw}=125$ μsec is added to the control loop,

b- The converter is modeled by a switching model,

c- The PWM sampling is modeled by a zero-order hold with sampling frequency of $f_s = 4\ kHz$.

d- The grid Thevenin impedance is $L_s = 460\mu H$, which corresponds to a normal SCR $=10$.

To illustrate the performance of the proposed controller, comparative analysis with the results of prevalent control scheme is provided. The prevalent control scheme parameters are given in (30). The control parameters for the proposed nonlinear controller are $k_{h1} = 2000, k_{h2} = 2000, k_{f1} = 1000, k_{f2} = 1000, k_{f3} = 1000$.

The power converter connects to the grid at $t = 0.2$ s, and to show the performance under different operating conditions, various P_{dc-2}s are applied in the range of $+P_{nom}$ to $-P_{nom}$ $(=\pm\ 100$ kW). Furthermore, DCLV reference is changed from 1100 V to 1150 V, and again is returned back to 1100 V. Also, the reactive power reference is changed from 0 kVAR to 20 and -20 kVAR and again to 0 kVAR consequently in both inverter and rectifier modes. The changes in the reference values and the related times can be seen in the corresponding figures. The further details of the simulations are provided in the following sub-sections.

5.1 Prevalent Controller

The simulation results including active and reactive power waveforms, the DCLV, and output currents are shown in Fig. 6. As shown in the figure, the system with the prevalent controller is stable in inverter mode $P_{dc-2} > 0$ with a proper time-domain response. However, in rectifier mode when $P_{dc-2} < 0$, the system response is deteriorated. Specifically, the system is unstable for $P_{dc-2} <$ less than $-80\ kW$.
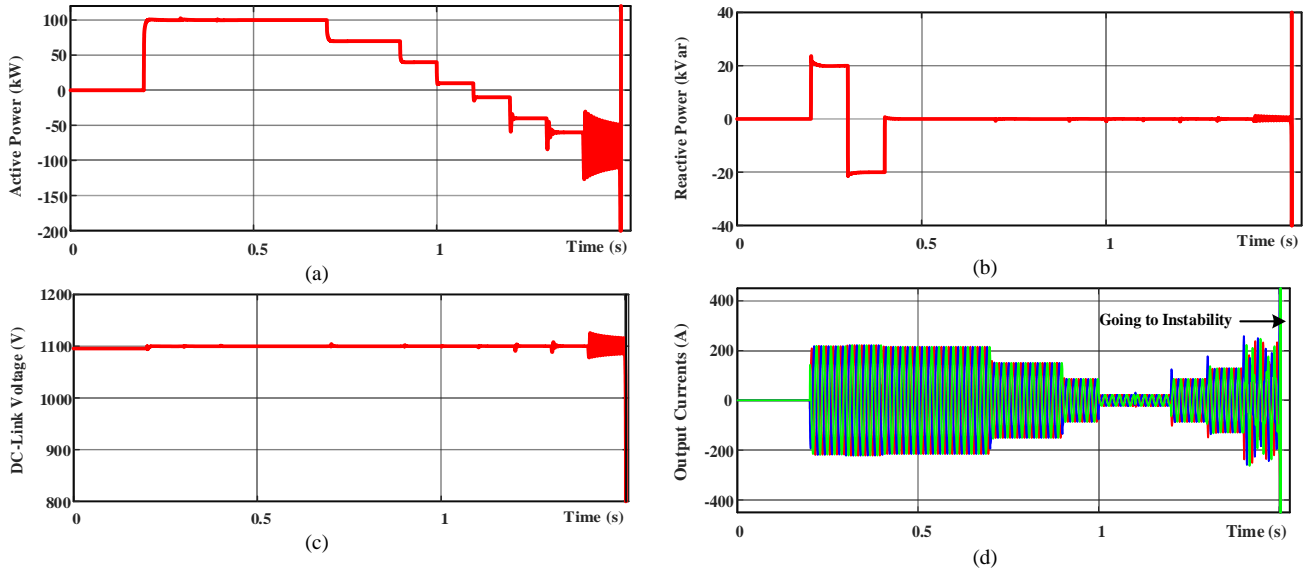

Fig. 6. Simulation results with the prevalent controller in (30): (a) active power, (b) reactive power, (c) DCLV, and (d) output currents.

5.2 Proposed Controller

In this sub-section, the performance of the proposed nonlinear controller is evaluated, and the results are shown in Fig.7. As shown in the figure, the system is stable in all operating points, and the reference commands are tracked with high speed and zero steady state error. The undershoot in the response of DCLV comes from the intrinsic non-minimum phase characteristic of the system which also exists in the prevalent control scheme. However, it does not have any adverse effect on stability margin of the system.

5.3 Proposed Controller with Uncertainties in the System Parameters

To show the performance of the proposed controller in presence of uncertainty in the system parameters, it is supposed that inductance of the output filter has been changed from $3mH$ to 2.5 mH, while the controller is designed based on $3mH$. The simulation results are presented in Fig.8. As it was expected, the presence of uncertainty has negligible effect on the system

dynamic response; and all expected criterion including high stability margin, fast dynamic response and accurate reference tracking are satisfied.
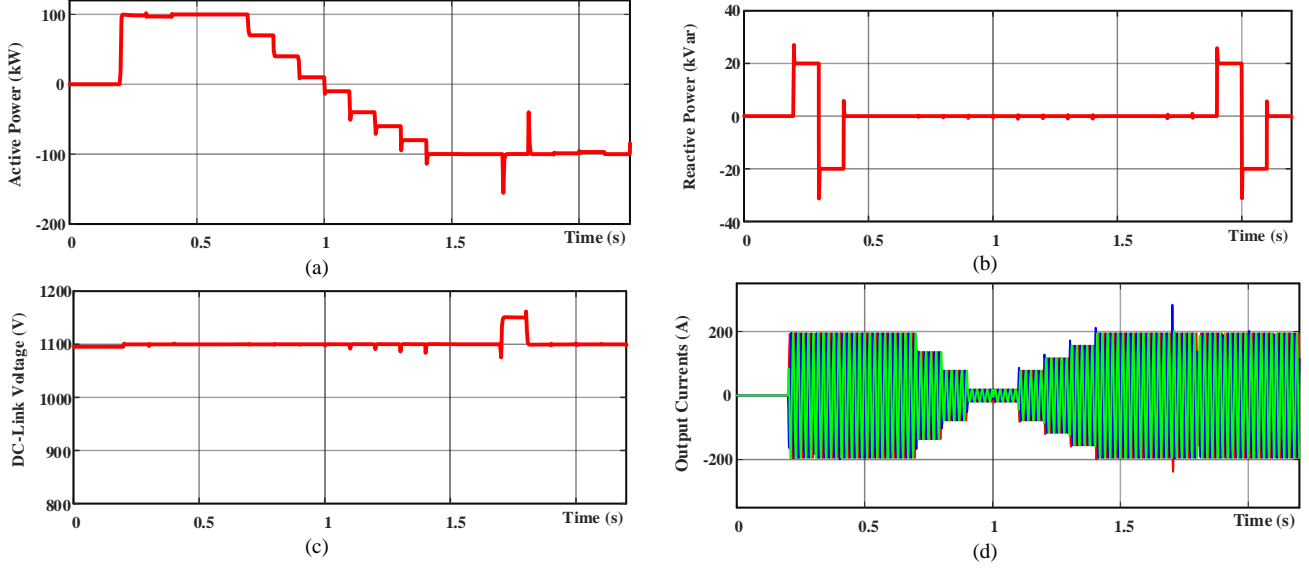

Fig. 7. System response with the proposed nonlinear controller: (a) active power, (b) reactive power, (c) DCLV, and (d) output currents.
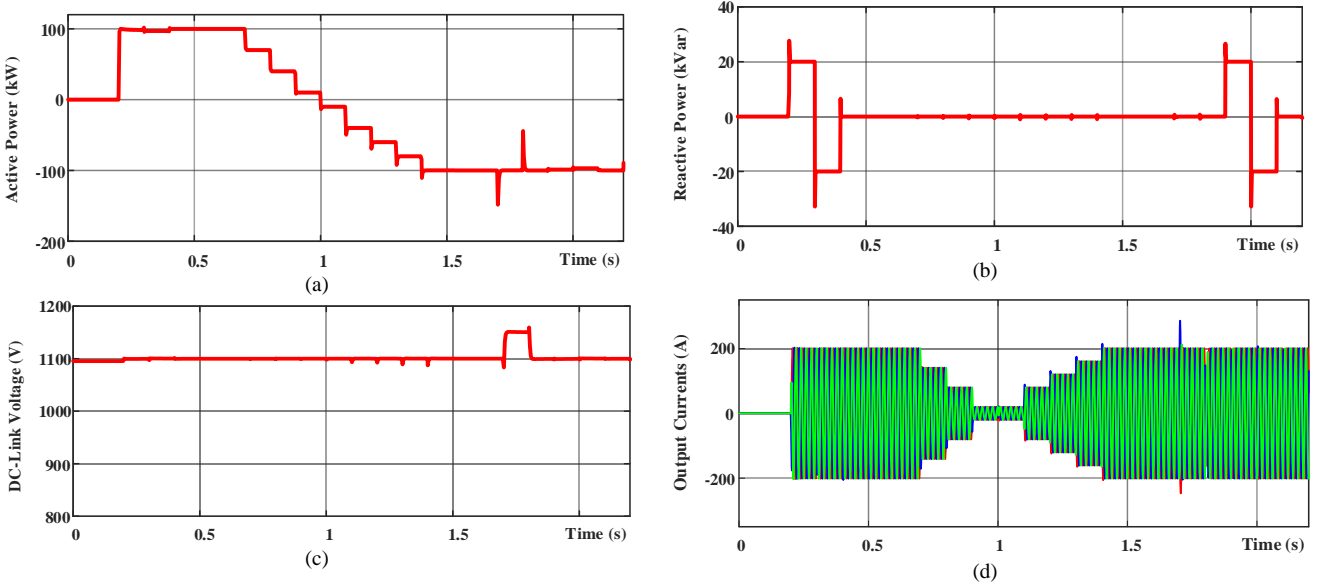

Fig. 8. System response with the proposed nonlinear controller in presence of uncertainty in filter inductance: (a) active power, (b) reactive power, (c) DCLV, and (d) output currents.

5.4 Proposed Controller in Short Circuit Fault Condition

As another scenario, to demonstrate the functionality of the proposed nonlinear controller to preserve the stability during large transients, two short circuit fault conditions are simulated. For the first fault condition, the converter is operating in the inverter mode by injecting 100 kW power into the grid. A three-phase short circuit occurs close to the converter at t= 0.3s, and cleared at t =0.4. This fault causes a voltage sag of about 70% at PCC. The second fault condition corresponds to rectifier mode of operation at $P_{dc-2} = -100 \, kW$, in which another three-phase short circuit fault occurs close to the converter busbar at t = 1.3s, and cleared at t = 1.4. This fault also leads to a voltage sag of about 70% at PCC. The simulation results are shown in Fig. 9. As shown in the figure, the stability of the system, including DC link voltage and grid current stabilities, are preserved in both fault conditions in inverter and rectifier modes. Furthermore, Fig. 9 (d) illustrates the dynamic response of DCLV during fault condition implying proper performance in case of severe voltage sag. It should be mentioned that the current of the VSC is limited to 205 A; hence, P_{dc-1} is limited and consequently P_{ac} decreases under short circuit fault conditions. It is worth to note that P_{dc-1} is supposed to be

limited by the primary source (in inverter mode) and DC loads (in rectifier mode), which it's used strategy details are beyond the scope of this paper.
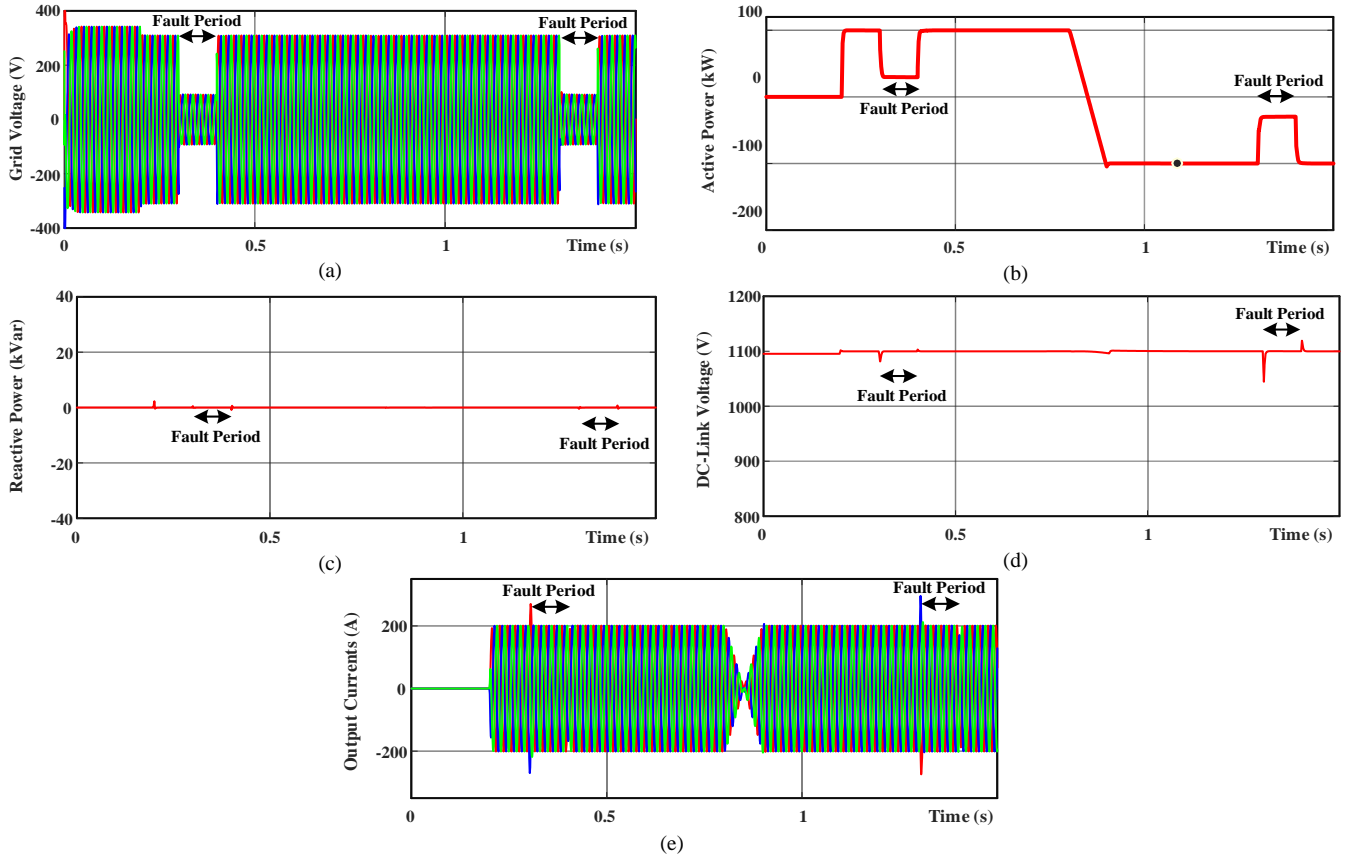

Fig. 9. System response with the proposed nonlinear controller in presence of grid fault in both inversion and rectification modes, (a) grid voltage, (b) active power, (c) reactive power, (d) DCLV, and (e) output currents.

6. CONCLUSION

This paper has explored the DC-link voltage (DCLV) stability of grid following Voltage Source Converters (VSCs) in bidirectional power flow applications. The prevalent DCLV control scheme, which is designed based on the simplified DCLV model, was analyzed in detail, and it was shown that due to ignoring the effect of output filter instantaneous power in controller design, the closed-loop system performance is not such as expected. Especially, the stability margin of the system decreases in the rectification mode with increasing the active power flow and DCLV control loop (BW_{dc}). This can threaten the stability and reliability of the overall power system. Limiting transfer power flow capacity is a simple remedy to preserve the stability of DCLV in rectifier mode operation, which decreases the VSC utilization factor. Also, decreasing BW_{dc} was another remedy, which, of course, degrades the system's performance. Although using the modified control design process based on the small signal model of DCLV, instead of the simplified model can improve the system stability, decreasing BW_{dc} is still necessary.

In order to address and resolve DCLV instability issue in VSCs, this paper, considering the non-linear dynamic of the BPCs and the interaction between dynamics of DC link voltage and AC currents, has proposed a non-linear controller based on combining the Lyapunov theorem and integral controller. It was proved that the stability of the converter in both rectification and inversion modes is preserved without any concern and limit from the side of DCLV control bandwidth and power level of the converter. As a result, the system can operate at both rectification and inversion modes, in the full power range, with high adjustable DCLV bandwidth, a suitable dynamic response, and high stability margin. Simulation results of various cases and comparison with the prevalent controller demonstrated theoretical findings and the effectiveness of the proposed nonlinear controller in terms of stability and robustness.

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