Data Branch Sharing Dual-Edge Explicit-Pulsed Level Converting Flip-Flops

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Abstract

Variable supply voltage-clustered voltage scaling (VS-CVS) is an effective way to decrease power consumption without compromising performance. One of the major challenges in VS-CVS design is that level converting flip-flops(LCFFs) not only need to have low power consumption but also high performance. In this paper, we propose two new structures of LCFF: the data branch sharing LCFF based on conditional charging (DBS-LCFFCC) and the data branch sharing LCFF based on precharging (DBS-LCFFP).The new structures adopt a data branch sharing scheme to improve the speed of the circuit as well as to reduce the number of transistors. Based on simulation results using HSPICE with PTM 32nm CMOS technology, the proposed LCFFs show an improvement of 19.2% to 67.2% and 41.6% to 76.3% in power-delay-product (PDP) at 50% data switching activity, respectively, compared to other advanced LCFFs.

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Abstract: Variable supply voltage-clustered voltage scaling (VS-CVS) is an effective way to decrease power consumption without compromising performance. One of the major challenges in VS-CVS design is that level converting flip-flops(LCFFs) not only need to have low power consumption but also high performance. In this paper, we propose two new structures of LCFF: the data branch sharing LCFF based on conditional charging (DBS-LCFFCC) and the data branch sharing LCFF based on precharging (DBS-LCFFP).The new structures adopt a data branch sharing scheme to improve the speed of the circuit as well as to reduce the number of transistors. Based on simulation results using HSPICE with PTM 32nm CMOS technology, the proposed LCFFs show an improvement of 19.2% to 67.2% and 41.6% to 76.3% in power-delay-product (PDP) at 50% data switching activity, respectively, compared to other advanced LCFFs.

Keywords: level-converting flip-flop; pulse triggered; low power; PDP

Introduction

With the development of very large scale integration (VLSI) systems, balancing power consumption and delay has become one of the biggest design challenges. The clock system is one of the most power-consuming parts of a VLSI system, accounting for 25% to 40% of total system power consumption [1]. Flip-flops are very critical parts of the clock system, so reducing the power consumption and delay of flip-flops has a profound impact on the total power consumption and delay of the entire VLSI system[2].

As power consumption is proportional to the square of the voltage, voltage scaling is the most effective way to reduce power consumption [3]. However, reducing the supply voltage causes an increase in circuit delay. Therefore, the variable supply voltage-clustered voltage scaling (VS-CVS) technique has been adopted for low-power systems. In this technique, the critical path is assigned to high supply voltage (VDDH) to maintain circuit performance, while the non-critical path is supplied with low supply voltage (VDDL) to reduce circuit power consumption. In the VS-CVS system, the high-voltage block can drive the low-voltage block directly. However, when the low-voltage block drives the high-voltage block, the PMOS transistor in the pull network on the high-voltage circuit cannot be fully closed, increasing the static power consumption. Therefore, when the circuits need to be connected with different supply voltages, it is necessary to employ a level converting flip-flop (LCFF) as an interface to complete the level conversion function [4-8].

Although several LCFFs have been proposed in the existing literature, there are still some drawbacks [9-13]. For instance, the required number of transistors is excessive, the power consumption is too large, and the delay is relatively high. To solve the above issues, in this paper we propose two data branch sharing dual-edge explicit-pulsed level converting flip-flops (DBS-LCFF). One of the DBS-LCFFs is based on conditional charging (DBS-LCFFCC) and the other DBS-LCFF is based on precharging (DBS-LCFFP). Based on data branch sharing technique, the proposed LCFFs can reduce the number of transistors and decrease the delay. Among them, DBS-LCFFCC can further reduce the power consumption, while DBS-LCFFP can further reduce the delay.

The rest of this paper is structured as follows. Section 2 reviews several existing level converting flip-flops. In Section 3, two novel data branch sharing level converting flip-flops are proposed. In Section 4, the proposed level converting flip-flops are simulated and compared with other flip-flops. Section 5 concludes the whole paper.

Previous level converting flip-flops Design

Compared to the master-slave structure level converting flip-flop, the pulse-triggered level converting flip-flop has a simpler structure and smaller delay. The pulse-triggered level converting flip-flop is divided into two types: implicit and explicit structures. The explicit structure has a smaller delay and can share a pulse signal generator with multiple flip-flops. This section mainly introduces several explicit pulse-triggered level converting flip-flops.

Fig. 1 shows the dual-edge triggered level converting flip-flop (DE-LCFF) [9], which is a dynamic flip-flop with node X precharged to VDDH by the full-swing pulse generated by the dual pulse generator. The input signal D, after passing through the sampling circuit, still needs to pass through two inverters to reach the output signal Q, which will cause a large delay. Another drawback is that when the input signal D keeps high, the dynamic power consumption is high due to the redundant switching activity of the internal node X. In addition, the DE-LCFF uses 33 transistors, which further increases the power consumption and area overhead.

The double-edge triggered level converter flip-flop with feedback (LCFFF) [10] is shown in Fig. 2. The LCFFF employs conditional discharge to reduce power consumption and the precharge technique to increase circuit speed. However, the pulse generator produces pulses differently at the rising and falling edges of the clock, resulting in asymmetry between the two pulses. This asymmetry may affect the stability of the circuit. In addition, the pulse generator requires large inverters to generate narrow pulses, resulting in significant power consumption.

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(a) (b)

Fig. 1. (a) Clock pulse generator; (b) Dual-edge triggered level converting flip-flop (DE-LCFF).

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(a) (b)

Fig. 2. (a) Clock pulse generator; (b) Double-edge triggered level converter flip-flop with feedback (LCFFF).

Fig. 3 shows the novel dynamic explicit-pulsed double edge triggered level converting flip-flop (nEP-DET-LCFF) [11], which removes the redundant switching activity of node X by using conditional discharge techniques to reduce the dynamic power consumption. However, the circuit's maximum NMOS transistor stack of 3, results in a long discharge branch for node X,, leading to a significant circuit delay. Moreover, the nEP-DET-LCFF requires more transistors than other designs, which increases the power consumption and area overhead.

The level converting flip-flop based on pass-transistor logic (LCFFBPT) [12] is shown in Fig. 4, which employs the feedback devices MP1 and MP3 to reduce the capacitive load (gate capacitance of the keeper device) at node V. However, when the input signal D changes from high to low during the presence of the pulse, the pull-up and pull-down branches of node V turn on simultaneously. Therefore, the pull-down branch needs to be strong enough to overcome the pull-up branch, which increases the power consumption and delay of the flip-flop.

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(a) (b)

Fig. 3. (a) Clock pulse generator; (b) Novel dynamic explicit-pulsed double edge triggered level con-verting flip-flop (nEP-DET-LCFF).

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(a) (b)

Fig. 4. (a) Clock pulse generator; (b) Level converting flip-flop based on pass-transistor logic (LCFFBPT).

Fig. 5 shows another proposed static level converting flip-flop (SLCFF) [12]. The SLCFF uses a small keeper transistor MP3 to prevent node X from becoming floated if the input signal D remains high during the presence of the pulse. Transistor MP1 is controlled by the input signal D. Node X remains low as long as the input signal D is high. However, this approach introduces a significant delay, even though it eliminates redundant switching activity at node X.

A novel double edge triggered level converter flip-flop (nDE-LCFF) [13] is shown in Fig. 6, which uses conditional data mapping technique to decrease redundant power consumption. However, the pulse generator in nDE-LCFF generates narrow pulses through transistors N1 and N2 on the rising edge of the clockand through transistor P1 on the falling edge, resulting in an asymmetry between the two pulses that may affect the circuit's stability. In Additionally, the pulse signal generator consumes relatively high power due to the use of large-sized transistors.

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(a) (b)

Fig. 5. (a) Clock pulse generator; (b) Static level converting flip-flop (SLCFF).

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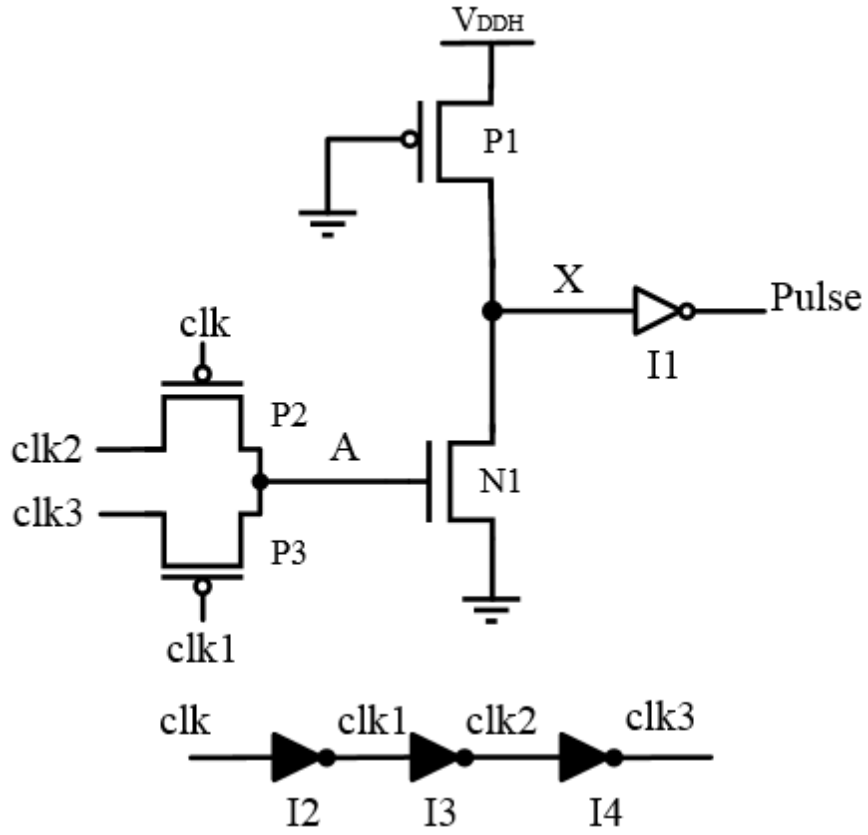
(a) (b)

Fig. 6. (a) Clock pulse generator; (b) Novel double edge triggered level converter flip-flop (nDE-LCFF).

Proposed level converting flip-flops

The existing level converting flip-flops have various problems, such as an excessive number of transistors, high power consumption, high delay, etc. Therefore, two level converting flip-flops are proposed in this paper to solve the above problems. This section mainly introduces the structure and working principle of the proposed level converting flip-flops.

The proposed duoble edge clock pulse generator is shown in Fig. 7(a) shows. It utilizes three cascaded inverters to generate delay signals CLK1, CLK2, and CLK3 from the clock signal CLK. Transistors P1 and P2 form a two-input transmission gate, where the clock signal CLK and its inverse delay signal CLK1 drive the gates of P1 and P2, respectively, and CLK2 and CLK3 serve as the two input signals of the two-input transmission gate. When CLK changes from "1" to "0", transistor P2 turns on, CLK2 remains "1", and node A outputs a high level to make transistor N1 turn on. Node X discharge to "0" by transistor N1, and then the pulse signal is generated by the inverter. After two inverter delays, CLK2 also becomes "0", transistor N1 turns off, and the pulse signal returns to the low level. When CLK1 changes from "1" to "0", transistor P3 turns on. The situation here is exactly similar to the above analysis, so we will not repeat it. The above discussion shows that the proposed pulse generator is a double-edge pulse generator with a pulse width of two inverter delays.



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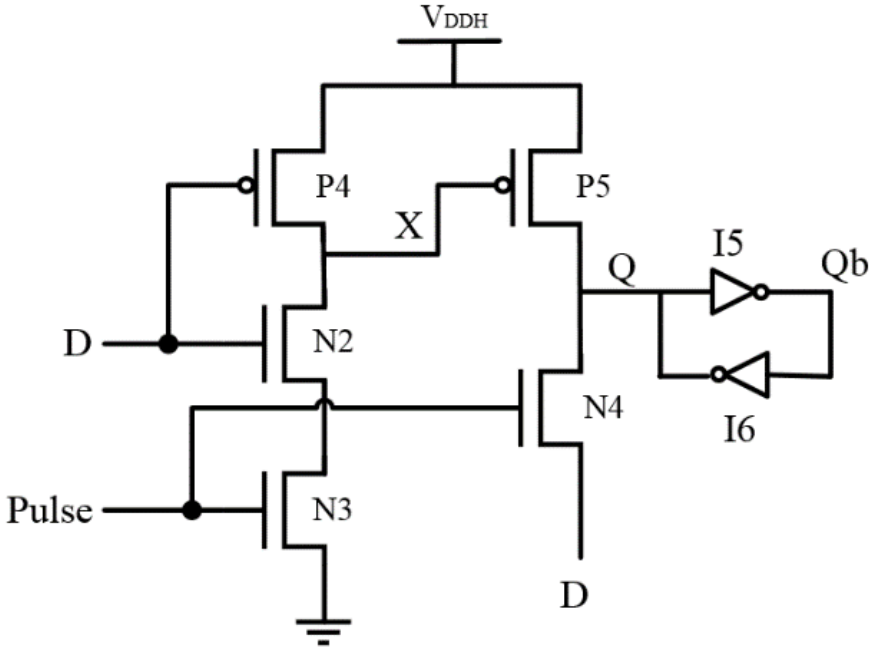

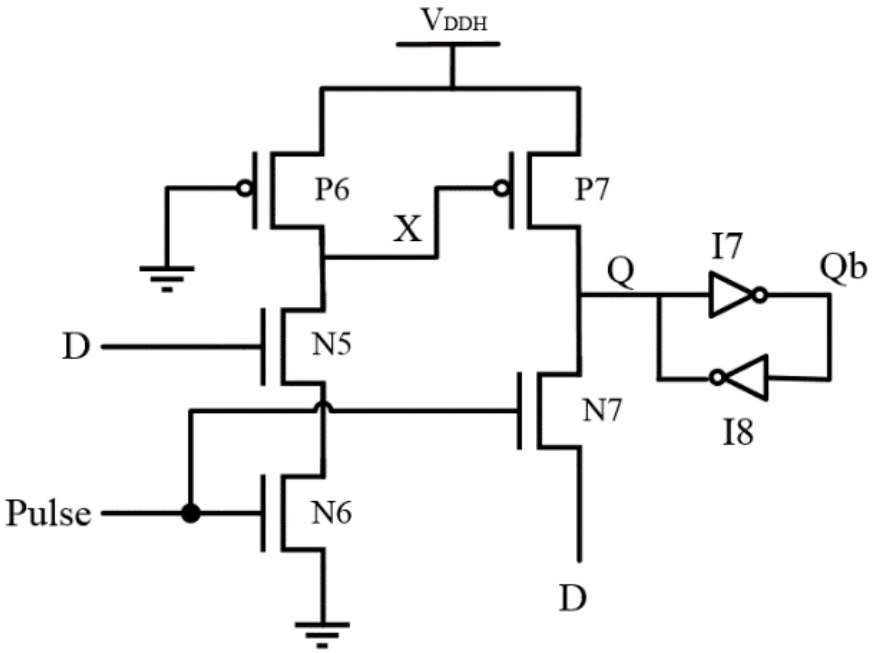

(b) (c)

Fig. 7. (a) The proposed clock pulse generator; (b) The proposed data branch sharing level converting flip-flop based on conditional charging (DBS-LCFFCC); (c) The proposed data branch sharing level converting flip-flop based on precharging (DBS-LCFFP).

Fig. 7(b) shows the proposed data branch sharing level converting flip-flop based on conditional charging (DBS-LCFFCC). The gates of transistors P4 and N2 are controlled by the input signal D. Therefore, the internal dynamic node X charge to "1" only when the input signal D is "0", at which time transistor P5 turns off. When the pulse signal arrives, transistor N4 turns on, and the output node Q discharges to "0" through transistor N4. When the input signal D is "1" and the pulse signal arrives, transistor N4 turns on, and the output node Q can charge to "1" through N4. In addition, the internal dynamic node X discharge to "0" as transistor P4 turns off and transistors N2 and N3 turn on. At this time, transistor P5 turns on and the output node Q can charge to "1" via P5. The charging and discharging paths of the output node Q are composed of a single transistor N4, which realizes the data branch sharing, reducing the number of transistors and further decreasing the delay of the circuit.

Fig. 7(c) illustrates the proposed data branch sharing level-converting flip-flop based on precharging (DBS-LCFFP). In contrast to the DBS-LCFFCC, the DBS-LCFFP has the gate of the pull-up network transistor P6 directly grounded for precharging the dynamic node X. As a result, when the input signal D changes from "1" to "0", the DBS-LCFFP does not need to turn on the pull-up network transistor P4 before charging the dynamic node X, which reduces the delay of the circuit. However, when the input signal D is "1" and the pulse signal arrives, the DBS-LCFFP generates additional short circuit power consumption due to a short circuit branch consisting of transistors P6, N5, and N6, which is not present in the DBS-LCFFCC. This is because the DBS-LCFFCC uses the conditional charging technique that avoids generating short circuit power. Therefore, the DBS-LCFFCC has lower power consumption, while the DBS-LCFFP has lower delay.

Simulation Results and Comparisons

The proposed LCFFs are simulated by HSPICE using PTM 32nm process technology. The simulation experiment employs two supply voltages, among which high supply voltage is 1.2V, and the low supply

voltage is 0.8V. The temperature is set to 25, the clock frequency is 125MHz, and the output load is a 10fF capacitor. Fig. 8 shows the simulation waveforms of the proposed LCFFs. Among them, the input signal D and the clock signal CLK employ a low supply voltage (0.8V). Q1 is the output signal of DBS-LCFFCC while Q2 is the output signal of DBS-LCFFP. We can observe from Fig. 8 that when the pulse signal is "0", the output signals Q1 and Q2 of the two LCFFs remain unchanged. When the pulse signal is "1", Q1 and Q2 collect the input signal D. Therefore, the proposed two LCFFs have the correct logic function.

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Fig. 8. The proposed LCFFs simulation waveform graph.

The proposed LCFFs are compared to the LCFFs presented in Section 2 in terms of performance.For the PTM 32nm process technology, all LCFFs are optimized to achieve the minimum power-delay product (PDP). The experimental conditions specified previously apply to this experiment. Table 1 shows the delay data for each LCFF obtained from the simulation. Among them, D—C— (or D—C—) denotes the minimum D-Q delay at the falling edge of the clock when the input signal D switches from "1" to "0" (or "0" to "1"). D—C— (or D—C—) denotes the minimum D-Q delay at the rising edge of the clock when the input signal D switches from "0" to "1" (or "1" to "0"). The average delay is the average minimum D-Q delay for the four cases.

Table 1. Delay comparison of various LCFFs

Flip-Flops	Delay of D-Q (ps)	Delay of D-Q (ps)	Delay of D-Q (ps)	Delay of D-Q (ps)	Average Delay (ps)
	D—C—	D—C—	D—C—	D—C—	
DE-LCFF	179.3	136.9	136.9	177.4	157.63
LCFFF	116.7	57.08	40.45	76.97	72.8
nEP-DET-LCFF	146.9	75.45	75.29	140.3	109.49
LCFFBPT	80.71	70.61	70.17	80.63	75.53
SLCFF	136.2	62.76	62.63	124.3	96.47
nDE-LCFF	110.3	68.1	50.29	84.46	78.29
DBS-LCFFCC	96.25	36.69	36.92	96.27	66.53
DBS-LCFFP	52.18	35.53	35.66	51.73	43.78

It can be seen from Table 1 thatthe two proposed LCFFs have a significant benefit in terms of delay. Among them, compared with the remaining six LCFFs, the average delay of DBS-LCFFCC decreases by 57.8%, 8.6%, 39.2%, 11.9%, 31%, and 15%, respectively, while the average delay of DBS-LCFFP decreases by 72.2%, 39.9%, 60%, 42%, 54.6%, and 44.1%, respectively. In addition, the delay of DBS-LCFFP is less than DBS-LCFFCC, which is consistent with our previous analysis.

These LCFFs were also simulated under different switching activities α to measure their power consumption, and the results are shown in Fig. 9. Fig. 9 indicates that the proposed DBS-LCFFCC has the lowest power consumption under arbitrary switching activities α because it adopts the conditional discharging technique and employs the minimum number of transistors. Furthermore, the power consumption of DBS-LCFFP is not as efficient when α is less than 50%, while it is only higher than the DBS-LCFFCC when the α is 100% because the extra short-circuit power consumption of the DBS-LCFFP outweighs the power savings from the transistors reduction when the switching activity is relatively low.

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Fig. 9. Power dissipation under different data switching activities

Table 2 presents a comparison of different LCFFs in various aspects, where the average power consumption and PDP are measured with α being 50%. Compared with other LCFFs, the PDP of DBS-LCFFCC decreases by 67.2%, 25.2%, 47.1%, 19.2%, 41%, and 29.9%, respectively, while the PDP of DBS-LCFFP decreases by 76.3%, 45.9%, 61.7%, 41.6%, 57.4%, and 49.3%, respectively. Although the power consumption of DBS-LCFFP is higher than the DBS-LCFFCC, it has a lower PDP due to the advantage of DBS-LCFFP in delay, which compensates for the loss in power consumption.

Table 2. Performance comparison of various LCFFs

Flip-Flops	Number of transistors	Hold time (ps)	Setup time (ps)	Average minimum D-Q delay (ps)	Average power (α=50%) (μW)	PDP (α=50%) (aJ)
DE-LCFF	33	-180.02	160.62	157.63	5.88	927.21
LCFFF	22	-280.2	90.78	72.8	5.58	405.94
nEP-DET-LCFF	32	-120.2	153.62	109.49	5.24	574.14
LCFFBPT	27	-130.2	150.62	75.53	4.98	376.23
SLCFF	28	-110.2	156.62	96.47	5.34	515.39
nDE-LCFF	22	-308.4	115	78.29	5.53	433.3
DBS-LCFFCC	21	-170.02	110.62	66.53	4.57	303.85
DBS-LCFFP	21	-150.02	80.62	43.78	5.02	219.82

In order to compare the influence of process–voltage–temperature (PVT) variations on the LCFFs, these LCFFs are simulated through different process corners, voltage and temperature. The results are shown in Fig. 10. It is obvious that the proposed DBS-LCFFCC gains power improvements in all five corners, while the proposed DBS-LCFFP gains delay improvements in all five corners. Moreover, the simulation results also show that the proposed DBS-LCFFCC has the lowest power dissipation as compared with others at different PVT variations, while the proposed DBS-LCFFP has the lowest delay as compared with others at different PVT variations.

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(a) (b)

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(c) (d)

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(e) (f)

Fig. 10. PVT variations effect on the LCFFs' performances: (a) process corners vs. power, (b) process corners vs. delay, (c) voltage vs. power, (d) voltage vs. delay, (e) temperature vs. power, (f) temperature vs. delay.

Conclusion

In this paper, we propose two types of double-edge pulse level conversion flip-flops based on data branch sharing , which can effectively reduce the number of transistors in the charge/discharge path and subsequently decrease the delay and area of the circuit. Among them, the DBS-LCFFCC employs the conditional charging technique to further decrease power consumption, while the DBS-LCFFP employs the precharging technique to further reduce delay. Simulation results show that both the proposed level-conversion flip-flops have lower power consumption and delay comparedto the existing level-conversion flip-flops.

Acknowledgments

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