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A 2.5 GS/s, 7-bit time-interleaved SAR ADC with real-time data output

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Abstract

This letter presents the design and measurement results of a 2.5 GS/s 7-bit successive approximation register (SAR) analog-to-digital converter (ADC) with real-time data output via the JESD204B protocol using two lanes at 12.5 Gb/s each. The ADC is implemented in a 22-nm fully-depleted silicon-on-insulator (FDSOI) technology and consists of four time interleaved ADC cores. It consumes 43 mW overall, while the analog frontend including the four ADC cores and the interleaver consumes only 7.8 mW. In the first Nyquist zone, the effective number of bits (ENOB) is larger than 6.1 bit leading to a Walden Figure-of-Merit (FOM_W) of 45 fJ/conv.-step and a Schreier Figure-of-Merit (FOM_S) of 150.5 dB. Integral (INL) and differential nonlinearity (DNL) are both well below 0.5 LSB for all measurement scenarios.

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This letter presents the design and measurement results of a 2.5 GS/s 7-bit successive approximation register (SAR) analog-to-digital converter (ADC) with real-time data output via the JESD204B protocol using two lanes at 12.5 Gb/s each. The ADC is implemented in a 22-nm fully-depleted silicon-on-insulator (FDSOI) technology and consists of four time interleaved ADC cores. It consumes 43 mW overall, while the analog frontend including the four ADC cores and the interleaver consumes only 7.8 mW. In the first Nyquist zone, the effective number of bits (ENOB) is larger than 6.1 bit leading to a Walden Figure-of-Merit (FOM_W) of 45 fJ/conv.-step and a Schreier Figure-of-Merit (FOM_S) of 150.5 dB. Integral (INL) and differential nonlinearity (DNL) are both well below 0.5 LSB for all measurement scenarios.

Introduction: Modern wireless communication as the 6th generation of mobile communication standard (6G) aim to achieve very high data rates e.g., as high as 1,000 GB/s [1]. On the other hand, power efficiency becomes the most critical point of handheld devices. Typical radio frequency (RF) frontends consist of analog pre-processing containing RF transmitter and/or receiver, and digital post-processing. In between, the signal is converted from analog to digital and vice versa. Talking about the RF receiver path, the analog-to-digital converter became one of the most power hungry components. Thus, high-speed and power efficient ADCs are strongly required these days. The resolution depends on the targeted application. In some cases, a very high resolution e.g., 24 bit, is required at the costs of a significantly lower speed and higher power consumption [2]. A moderate resolution of 7 bit is a good compromise for many applications, like phase modulated continuous wave (PMCW) radar systems [3]. However, even for 7 bits, ultra-fast flash-ADCs, as demonstrated e.g., for 24 GS/s with 3 bit resolution [4], require high number of comparators and, hence, large chip area and consume much power. Recently, we demonstrated an 8-bit successive approximation register (SAR) ADC consuming only 1.73 mW at a maximal sample rate of 1.25 GS/s [5]. More recently, we also designed and measured a 7-bit ADC with an even higher speed of 1.7 GS/s while consuming only 1.38 mW [6]. However, the requirements of even higher data rates with a very low power consumption at the same time, can barely be fulfilled using single-core ADCs rather than advanced concepts like time interleaving (TI) of multiple ADC cores. In this work, we describe a time interleaved SAR ADC consisting of four ADC cores. A real-time data output is implemented using the JESD204B readout interface. This interface with two lanes each operating at 12.5 Gbit/s is well suited for a broad range of applications with the ADC being integrated in a larger system.

Circuit Description: To prove the concept of the a TI SAR ADC with real-time data output, it was designed and manufactured using a 22-nm fully-depleted silicon-on-insulator (FDSOI) technology. The schematic of the 4× TI ADC is shown in Figure 1. It consists of four SAR ADC cores based on the alternating-comparator concept. In this letter, we focus on the description of the interleaver system. The ADC contains mainly five different components: 1) an input-matching network for the differential inputs. 2) a bootstrap sampling switch as well as two 45-fF sampling capacitors as track-and-hold unit, 3) a reset switch shorting both differential inputs for a short, well defined period, 4) a buffer amplifier decoupling the input network from the high capacitive load of the ADC cores, 5) the four ADC cores. The ADC is clocked with a 2.5 GHz clock generated by a clock divider using an external 12.5 GHz clock also utilized for the JESD20B interface. This clock is further divided by four and shaped in another building block (clock generation) as shown in the second large building block from the top. Here, the reset signal mentioned above is generated as well. Additionally, another clock divider by factor two is used to generate a 6.25 GHz clock for the real-time readout using JESD204B. The clocking structure of the ADC was carefully optimized to ease the implementation of the JESD204B interface. We used two output lanes, each providing a data rate of 12.5 Gbit/s to achieve a real-time data output (up to 25 Gb/s). As mentioned above, the 12.5 GHz input clock to the chip is divided by 5 also to generate the ADC clock: Doing so, only a single clock signal needs to be supplied to the chip. Thus, no synchronization between different clock domains is needed, massively simplifying the design of the JESD204B interface. The timing diagram is shown at the bottom of Figure 1. As can be seen, all four ADC cores are activated successively and the input clock is shaped to a duty cycle of 25% ($clk_{smpl,master}$). Furthermore, a serial periphery interface (SPI) is implemented and used to configure the chip. As it is a time interleaved ADC, mismatch between the individual ADCs can cause impurities in the spectrum. For that, a gain calibration is included, such that the reference voltage for each of the four sub-ADCs can be set individually with 10 bit accuracy. The offset of the comparator is calibrated in background within each sub-ADC. The data are send via the real-time JESD204B transmitter with two lanes as mentioned above and a limited number of values is additionally stored in on-board memory.

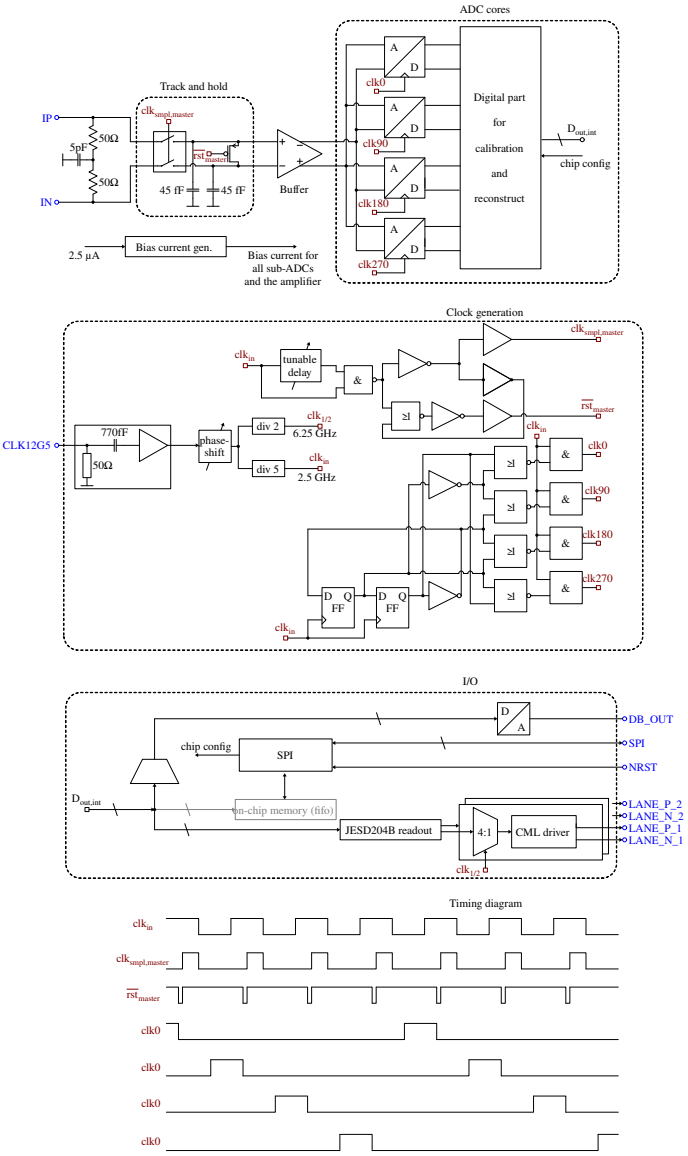

Fig 1 *Block diagram of the entire testchip including I/O and details to clock generation.*

Measurement Setup: The measurement setup is shown in Figure 2. The chip is bonded to a printed circuit board (PCB) to form the device-under-

test (DUT) as shown in Figure 3. The overall chip size including pads, I/O cells, and memory is approximately 1 mm^2 while the analog frontend including the four ADC cores, the interleaver, and the real-time data output occupies only approximately 0.10 mm^2. Two sine wave sources were used to generate the input and clock signals for the ADC. For the input signal, a balun and bias tees were used to generate the required differential signal. A measurement was started with a positive SYSREF pulse generated by a waveform generator. This enables the real-time data output of the ADC chip and on the same time triggers the real-time oscilloscope (Keysight UXR-0702AP) to capture about 10 µs of the JESD204B bitstream. The captured data of the scope were then transferred to a PC, where the JESD204B decoding takes place and the ADC data is evaluated (e.g., calculation of the spectrum). An SPI is used to configure the chip as mentioned above. Thus, a 0.8 V-to-3.3 V levelshifter PCB is required (cf. Figure 3). To adjust the supply voltages of I/O cells, ADC core, interleaver, and digital part separately and monitor the power consumption of each block, four different supply voltages were used all in the range of 0.7 V and 0.9 V.

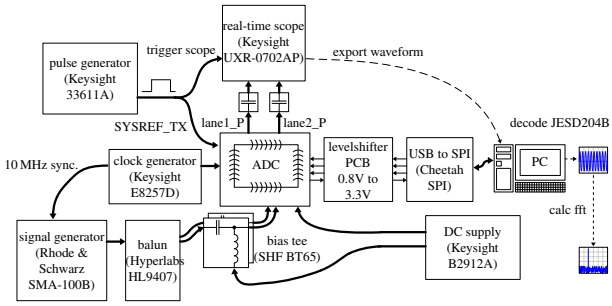

Fig 2 *Block diagram of the measurement setup.*

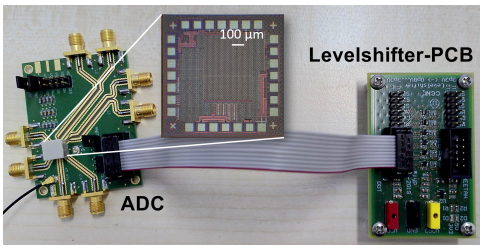

Fig 3 *Microphotograph of chip and PCB used for the measurements.*

Measurement Results and Discussion: The spectra were calculated using the decoded waveforms from the JESD204B bitstream. As can be seen in Figure 4.a, the spurious-free-dynamic range (SFDR) of 53.5 dB is reached at low input frequencies, where the largest harmonic is located at $f_{clk}/4$. As these tones are well below the achieved signal-to-noise-and-distortion ratio (SNDR), the ADC is noise limited at low input frequencies and the distortions do not have a significant impact. Figure 4.b and Figure 4.c show further spectra near the Nyquist frequency and near a 12.5 GHz input frequency. The performance is mostly equal at the Nyquist frequency, showing the good performance of the ADC. Even at 10 times the Nyquist frequency (10×1.25 GHz), the SFDR is above 34 dB. The noise floor is a little higher at 12.5 GHz due to the clock jitter, which is much more severe at the high input frequency. As a summary, Figure 4.d shows the measured SNDR and SFDR versus the input frequency for the whole band of interest. From the SNDR, the effective number of bits (ENOB) at fullscale (FS) input can be calculated using the well-known equation

$$ENOB = \frac{SNDR - 1.76}{6.02}. \quad (1)$$

The calculated ENOB is depicted in Figure 4.e. It is above 6.1 bit at low input frequencies (for the first Nyquist zone) and degrades towards higher input frequencies due to noise (jitter) and spurs. Up to 2 GHz input frequency (above Nyquist), the ENOB stays above 6 bit and up to 6 GHz the ENOB is still above 5 bit. At the highest input frequency of 12.5 GHz, the ENOB degrades to 4.5 bit, which is still a remarkable value considering the sample rate of only 2.5 GS/s. Finally, the static nonlinearity of the ADC is measured as depicted in Figure 4.f with the histogram-based method and a sine-wave input at low frequency. The integral (INL) and differential nonlinearity (DNL) are well below 0.5 LSB. Thus, the static nonlinearity does not limit the ADC. The power consumption of approximately 43 mW divides as follows: the power dissipation of the digital part of 20.6 mW is dominating the chip. It is needed for the JESD204B readout circuitry and the leakage current for the on-chip memory. The I/O supply is used mostly for the common mode logic (CML) driver outputs as well as for the clock input buffer. The power consumption of the ADC itself (cores and interleaver) is just 7.8 mW. In the first Nyquist-zone (ENOB >6.1 bit) the ADC achieves a Walden Figure-of-Merit (FoM$_W$) of 45 fJ/conv.-step and a Schreier Figure-of-Merit (FoM$_S$) of 150.5 dB.

Comparison with State of the Art: The presented ADC compares well with state-of-the-art devices. However, some recent works demonstrated also remarkable results, especially those using heavily interleaved SAR ADCs. Two examples using with 64× are the work of Seual et al. [7] and Liu et al. [8] both presented in 2022. In [7], an extremely high sample rate of 112 GS/s was achieved, but the overall power consumption was quite high with 315. 2 mW and 189.1 mW overall and for the ADC only, respectively. In [8], a very effective 10 GS/s ADC was presented providing a FoM$_W$ of 24.6 fJ/conv.step and a FoM$_S$ of 152.6 dB. Both of these works utilized an advanced 5 nm CMOS process, which offers very good conditions for high-speed digital design as well as area and power efficiency. On the other hand, however, analog and RF design remains challenging in this technology and the costs are still very high. We used an established 22 nm FDSOI technology, which also provides good capability for fast and power-efficient digital design and, additionally, is one of the best choices for RF design as demonstrated in several works e.g., [9][10][11]. Hence, a monolithic integration of the RF frontend and high-speed ADC is feasible in this technology and, thus, probably better suited for the latter application. Furthermore, our design offers a real-time data output via JESD204B, what was not shown in the above mentioned works. Here, another interesting recent example representing the state of the art is a 50 GS/s TI-ADC with real-time data output [12]. Still, in this case the power consumption is as high as 894 mW, which is approximately 100 times higher than the power consumption of our ADC, while the speed is only 20 times higher. Still, this is also an impressive work and it utilizes an older 40 nm technology and 128× TI. In our design, the sample rate per ADC core is higher compared to [8][12] and the power efficiency per ADC core is lower compared to [7][12] and we expect a sampling rate of 40 GS/s and 80 Gs/s with a power consumption of approximately 150 mW and 300 mW for future 64× and 128× TI, respectively.

Conclusions and Outlook: We designed and measured a high-speed (2.5 GS/s) time-interleaved 7 bit SAR ADC with a power consumption of 43 mW while the ADC itself consumes only 7.8 mW using an established 22 FDSOI technology also well suited for RF design. Despite to the majority of the previous works, this chip includes a real-time data output via JESD204B. Simulations and previous measurements on single-core test chips suggest that this type of 4× TI ADC should be able to achieve even higher data rate of up to 5 GS/s with an only slightly higher power consumption, but in this case the I/O interface has to be adjusted and real-time readout would be more challenging. In the future, we will implement TI-ADC consisting of more ADC cores (e.g., 16). In this case, we expect sampling rates of up to 24 GS/s with a power consumption of approximately 35 mW. Additionally, we will further optimize ADC core and interleaver and interleave even more cores as discussed in the previous section.

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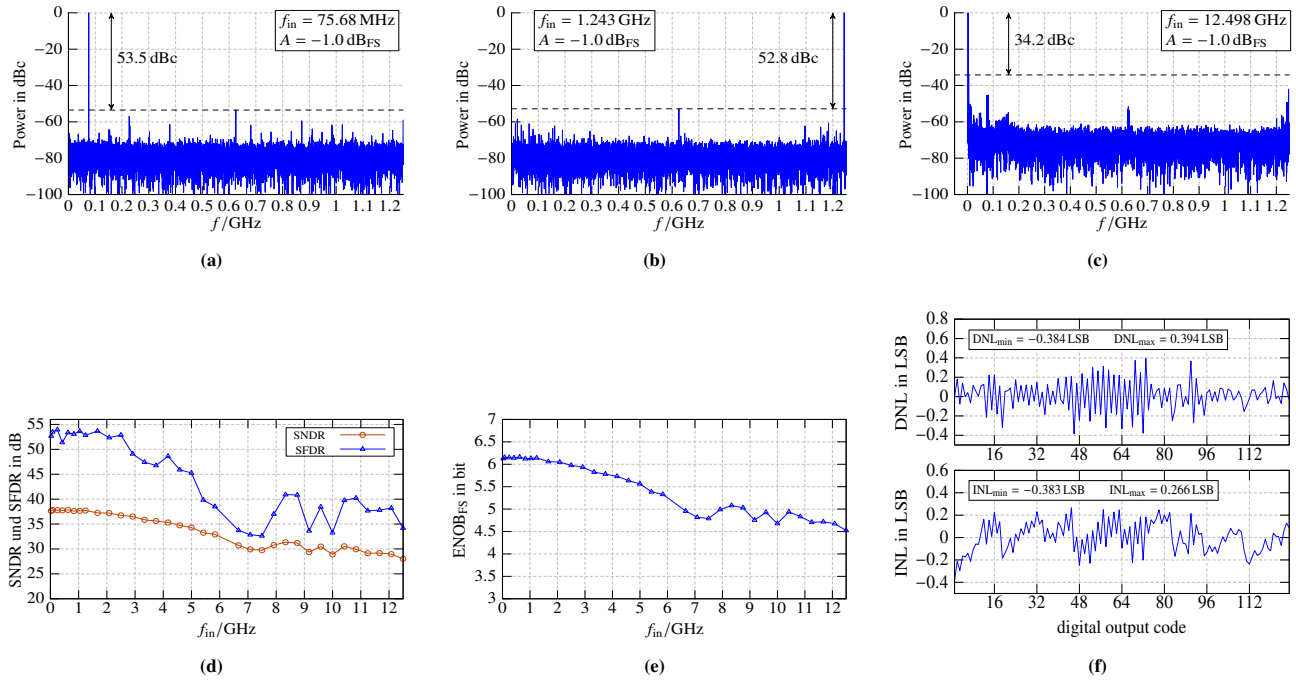

Fig 4 *Measurement results: spectra for different input frequencies and sample rate of 2.5 GS/s (a-c), SFDR, SNDR (d), ENOB (e) against input frequency and static nonlinearities INL, DNL (f).*

Table 1. Comparison with state of the art

Ref., year	f_S[a] (GS/s)	Resolution (ENOB[b])	Power (mW)	FoM$_W$ (fJ/c.s.[c])	Readout interface	Type	Core area (mm^2)	FOM$_S$ (dB)	Technology
[4] 2016	24	3 (2.2)	410	3607	real-time (only 3b)	Flash	0.12	119.7	28 nm FDSOI
[5] 2022	1.25	8 (6.86)	1.73	11.9	on-chip mem., SPI	SAR	0.0025	158.6	22 nm FDSOI
[12] 2021	50	8 (5.82)	894	317	real-time 16-lane TX	128× TI SAR	1.232	142.3	40 nm FDSOI
[7] 2022	112	6 (4.5)	189.9[d] (315.2)	75.9	- (64K PAM-4)	64× TI SAR	0.34	143.6	5 nm CMOS
[8] 2022	10	8 (5.82)	14.8	24.8	-	64× TI SAR	0.0029	152.6	5 nm CMOS
This 2023	2.5	7 (6.1)	7.8[d] (43)	45.4	JESD204B	4× TI SAR	0.10	150.5	22 nm FDSOI

[a] f_S: sample rate [b] near Nyquist [c] c.s.: conversion step [d] power consumption of analog frontend

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