An Ultra-Low-Power Reconfigurable Power-On Reset for Multi-Supply Voltages Applications

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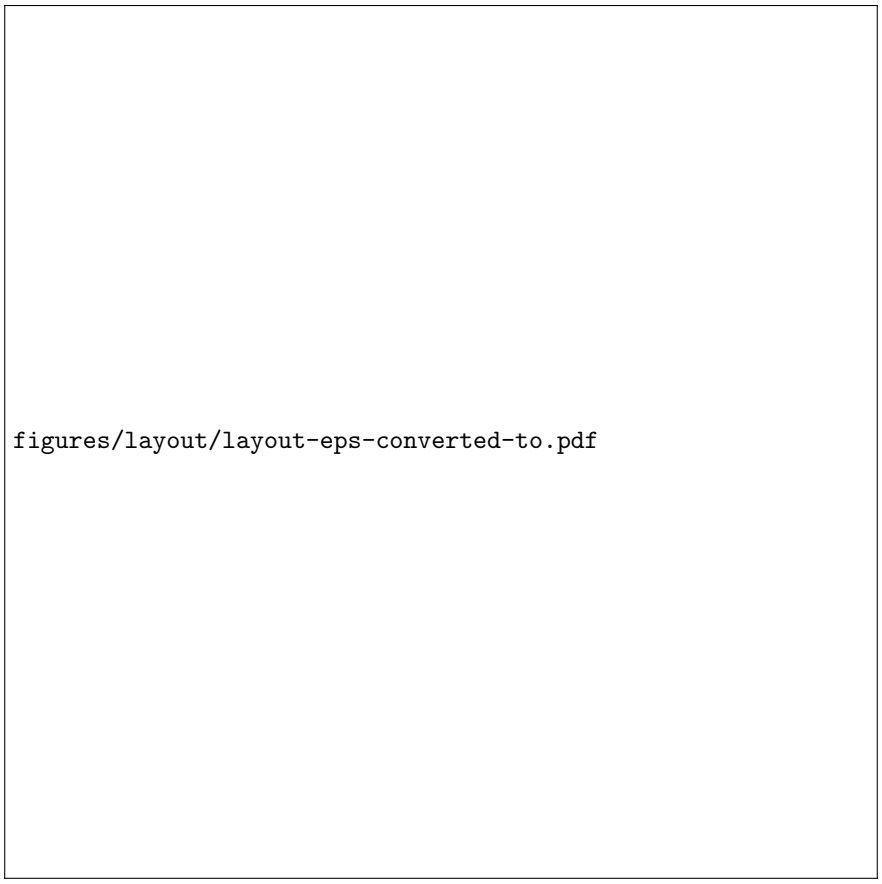
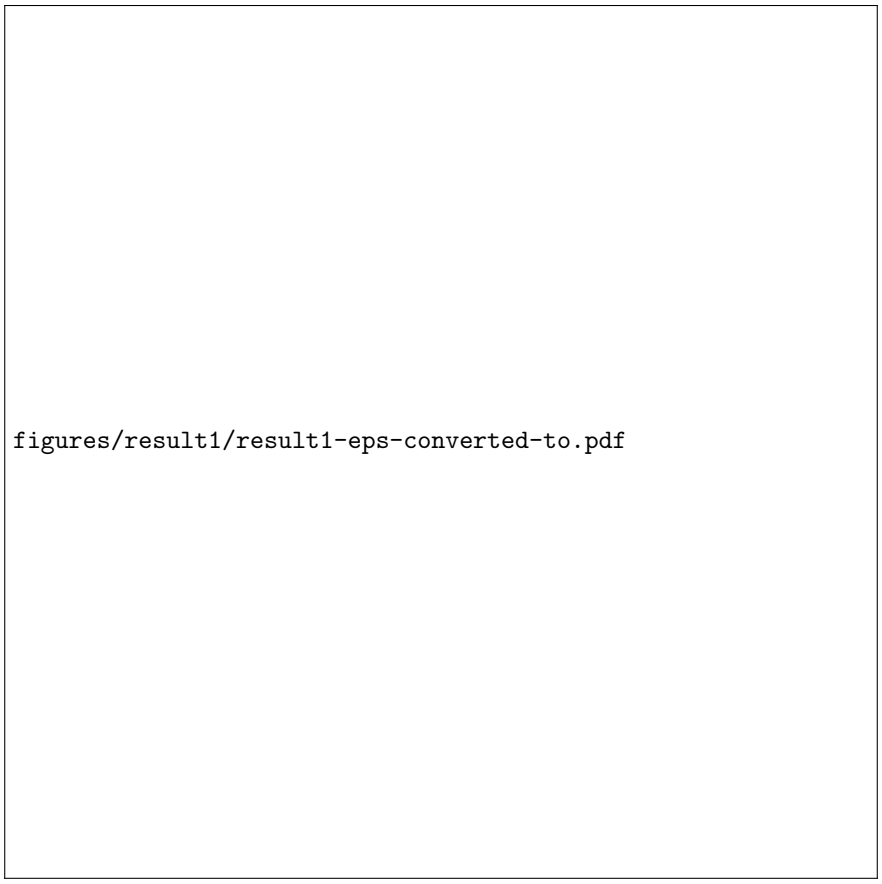
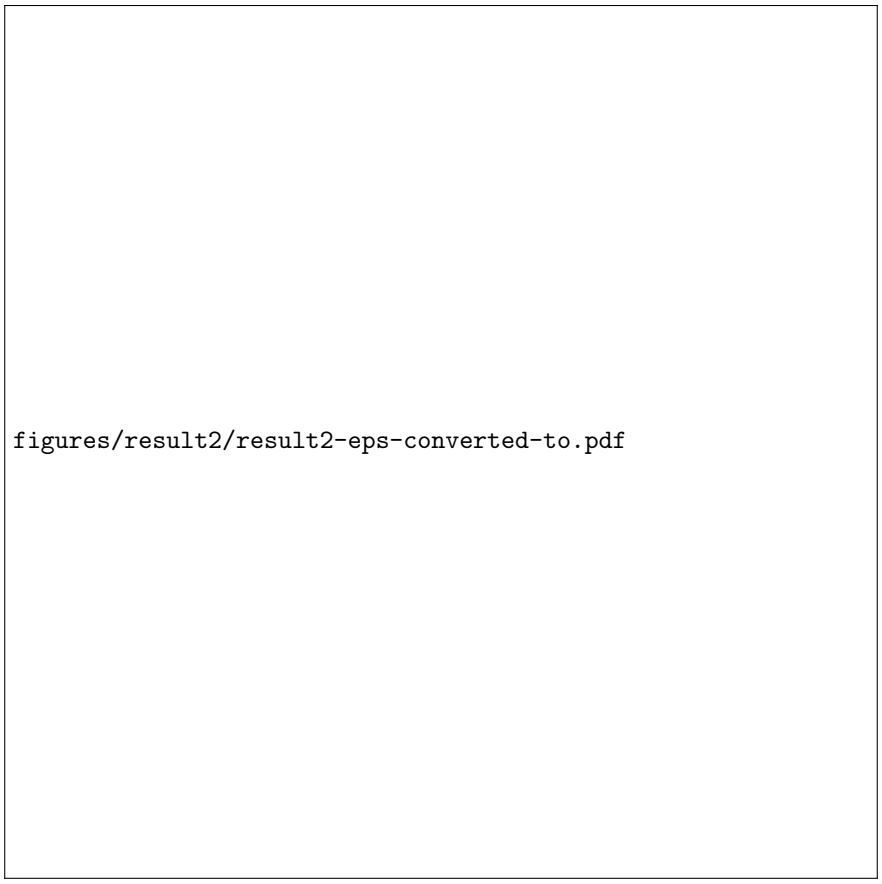
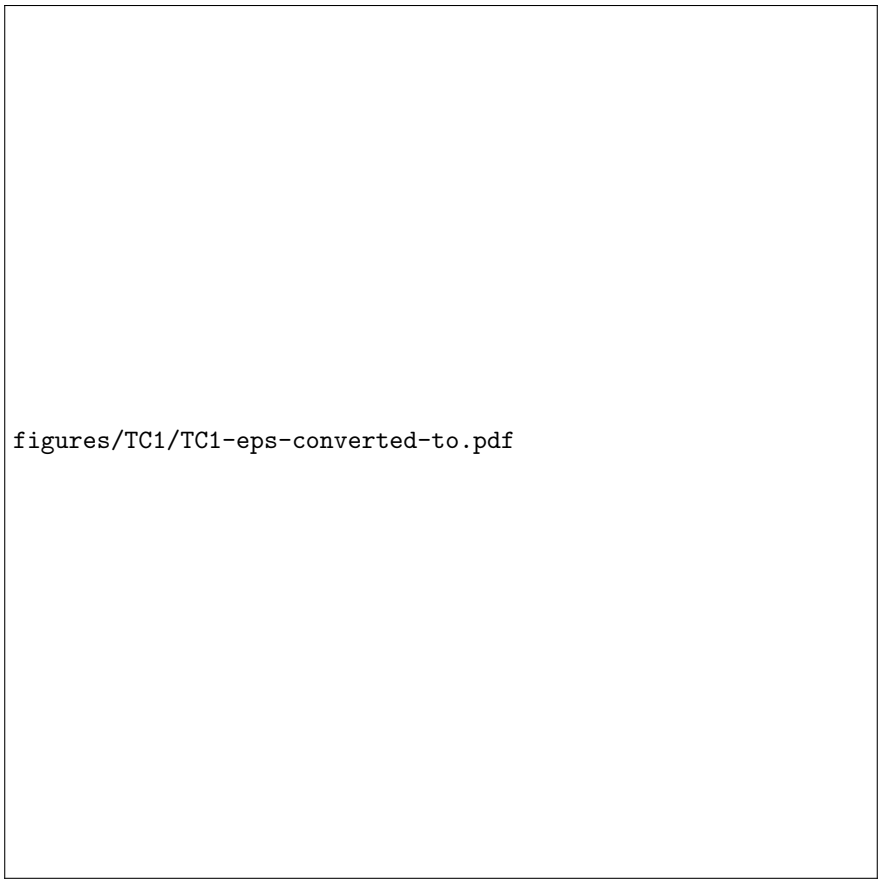
Abstract

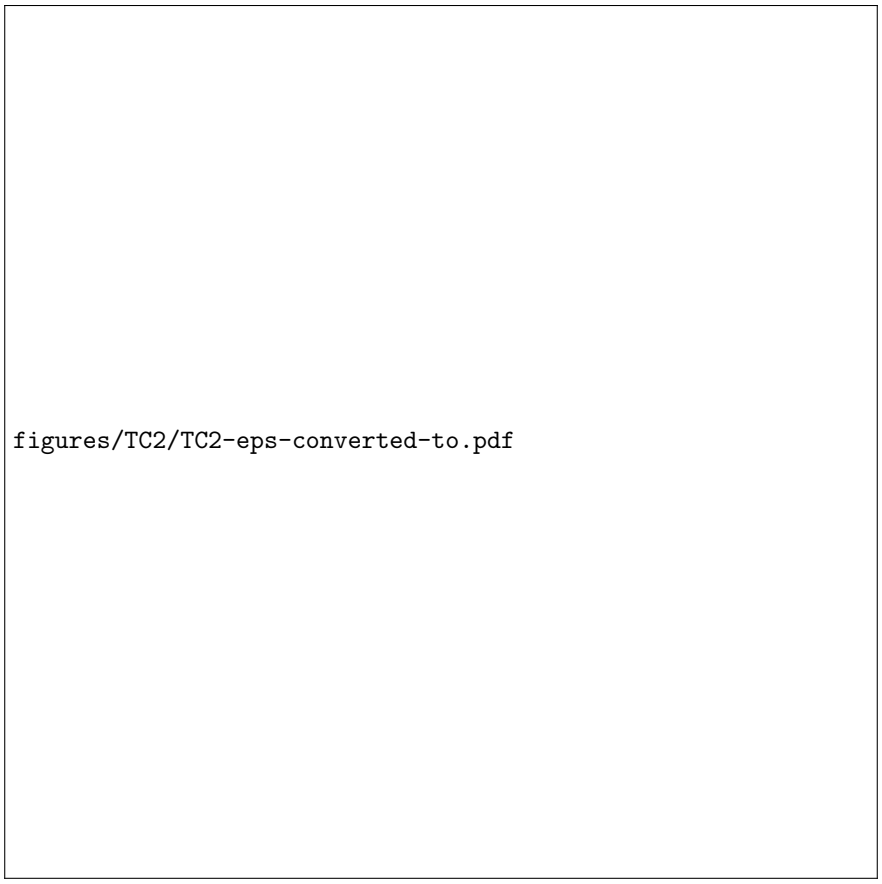
In this letter, an ultra-low-power power-on-reset circuit with reconfigurable trip-voltages is proposed. In order to reduce area and power consumption overhead, an all-MOS sub-threshold architecture based on threshold difference voltage references and current comparator is designed. By configuring the reference current and the different threshold transistors, the different trig voltages are generated to detect multi-supply voltages. Simulation results based on 55 nm CMOS process show that the proposed power-on-reset circuit generates trip voltages of 385.5 mV and 775.4 mV, consuming only 8.5 nA and 92.6 nA at the supply voltage of 0.5 V and 1 V, respectively. And the area of the proposed power-on-reset circuit is as low as 240 μm^2.

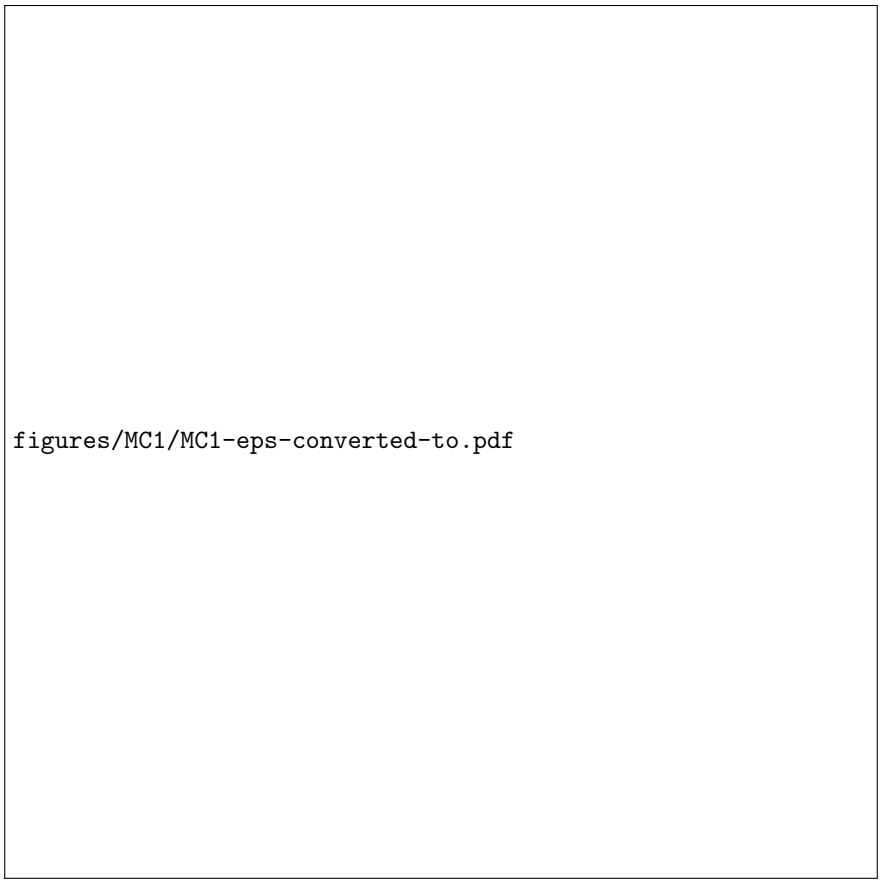


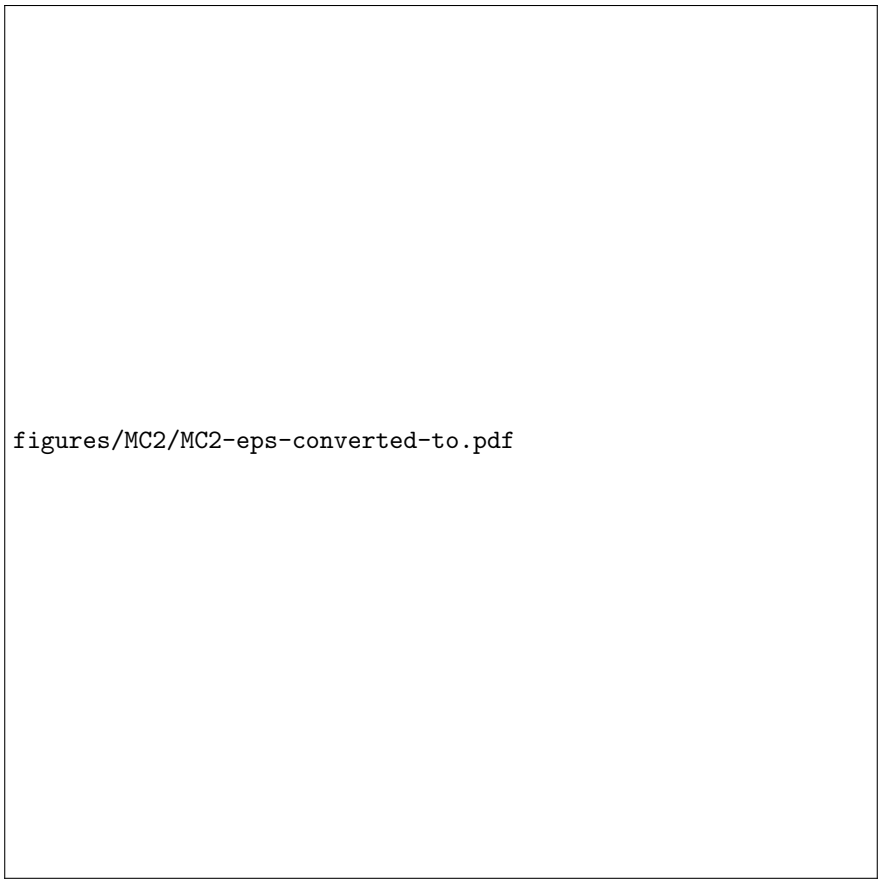


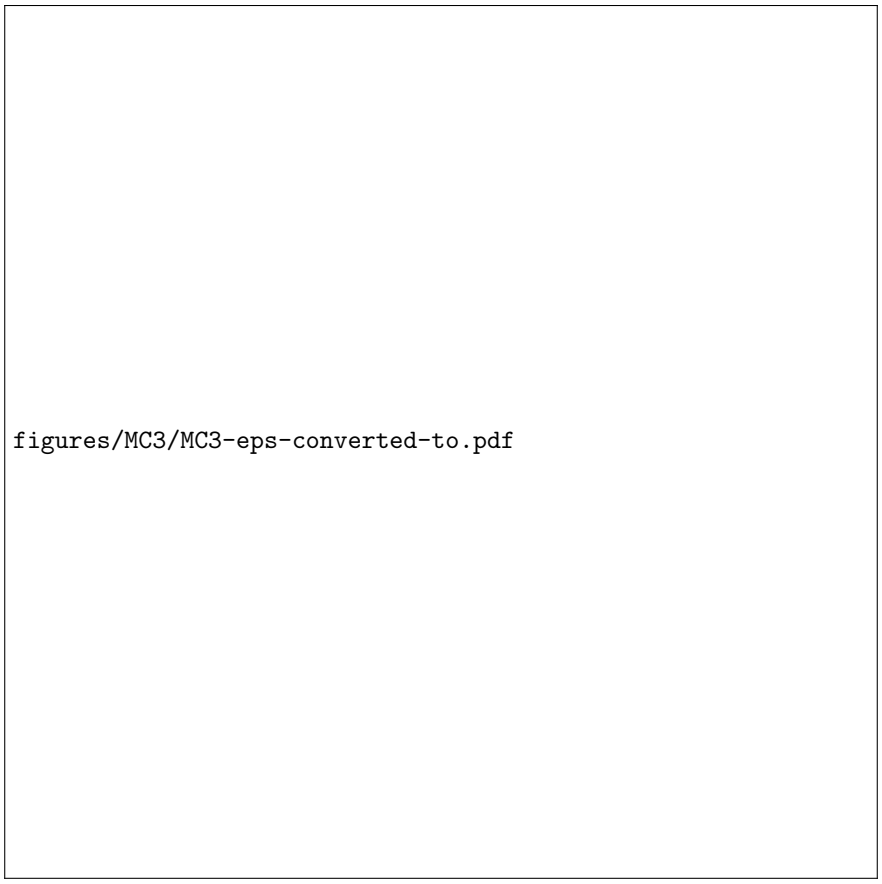


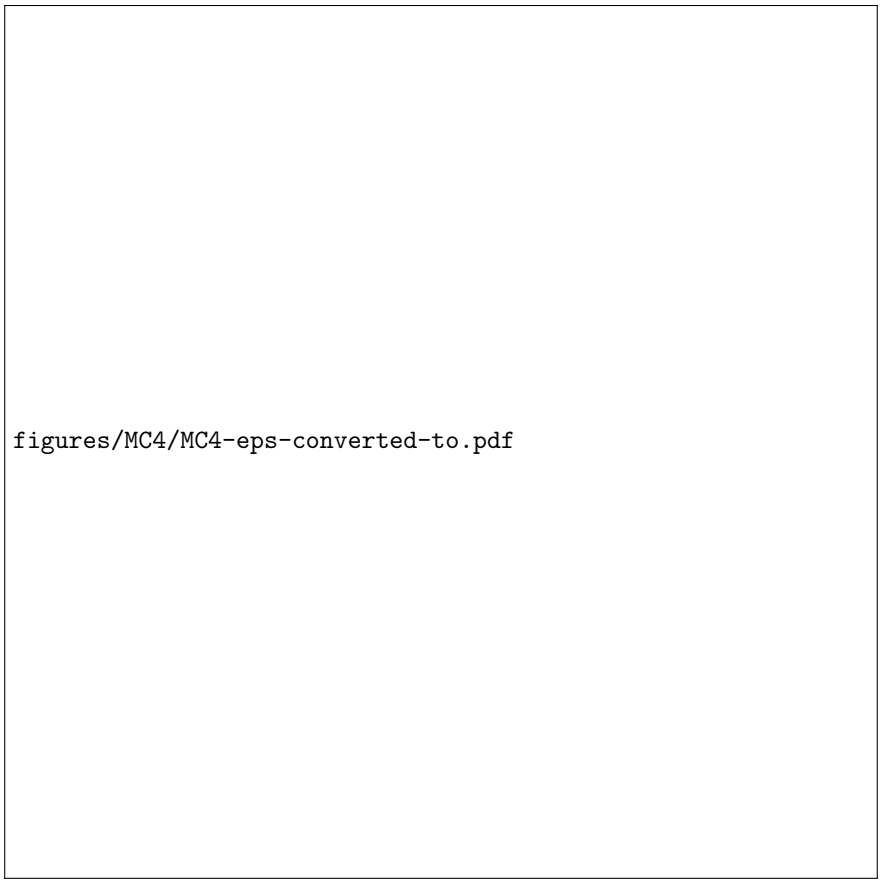












An Ultra-Low-Power Reconfigurable Power-On Reset for Multi-Supply Voltages Applications

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In this letter, an ultra-low-power power-on-reset circuit with reconfigurable trip-voltages is proposed. In order to reduce area and power consumption overhead, an all-MOS sub-threshold architecture based on threshold difference voltage references and current comparator is designed. By configuring the reference current and the different threshold transistors, the different trig voltages are generated to detect multi-supply voltages. Simulation results based on 55 nm CMOS process show that the proposed power-on-reset circuit generates trip voltages of 385.5 mV and 775.4 mV, consuming only 8.5 nA and 92.6 nA at the supply voltage of 0.5 V and 1 V, respectively. And the area of the proposed power-on-reset circuit is as low as 240 μm^2.

Introduction: Modern high-performance microprocessors usually require different functional modules working in individual domains to maximize the performance and reduce power dissipation [1]. To avoid the floating states of memory and registers in digital system causing undesired initial behavior during the ramp-up [2], a power-on-reset (POR) circuit with brown-out-reset (BOR) function is needed to ensure them a known or initial-state behaviour. Since there are multi-supply voltages (MSV) generated for digital systems by power management units [3], several POR circuits will be widely used to monitor different supply voltages. As Figure 1 shows, multiple POR circuits may be used to detect the state of different supply voltages to produce respective reset signals RSTN, which remain low before the supply voltages reach their own POR trip-voltages (VPOR) and will be released to follow the power when the supply voltages exceed their VPOR. Meanwhile, the reset signals return to low once the supply voltages drop below their BOR trip-voltages (VBOR). And hysteresis window is defined as the difference between VPOR and VBOD, which is used to avoid RSTN glitches caused by power jitters. Traditional POR architectures broadly adopt delay-based scheme [4, 5] or bandgap-based scheme [2, 6]. The bandgap-based POR circuits consisting of a bandgap and a voltage comparator usually consume several uA to obtain high accuracy trip voltage. The delay-based POR circuits consisting of a current source and a capacitor only consume nA quiescent current while the trip-voltage is very sensitive to PVT variations. In addition, BJTs, resistors or capacitors used in above two type POR circuits consume area overhead in compact system applications.

In this letter, we propose an ultra-low-power all-MOS POR circuit to meet the requirement of detecting the multi-supply voltages. Based on the voltage threshold difference (ΔVth) voltage reference (VR) scheme [7–9], a reference current and a Vdd-tracking current are compared by a current comparator to generate the different accurate reset signals with a small cost of area and power consumption. Using the different voltage threshold MOS transistors, the proposed POR circuit has realised configurable trip voltages without additional circuit complexity, which are crucial in MSV systems.

Proposed POR architecture: As shown in Figure 2, the proposed POR circuit consists of three parts, a 3-transistors (3T) VR, a Vdd-tracking VR and a scalable current comparator. The native device MN0 and two same I/O devices MN1 and MN2 form the 3T VR to bias the core device MN3 to generate the reference current I1. Meanwhile, two core devices MP3 and MP4 work as a Vdd-tracking VR to bias the optional MN4 (the core device MN4L or the I/O device MN4H) to generate the Vdd-tracking current I2. A current mirror composed of MP1 and MP2 in the current comparator are used to replicate the current I1 and compare I2 with it. The number of MN3 and device type of MN4 make the current

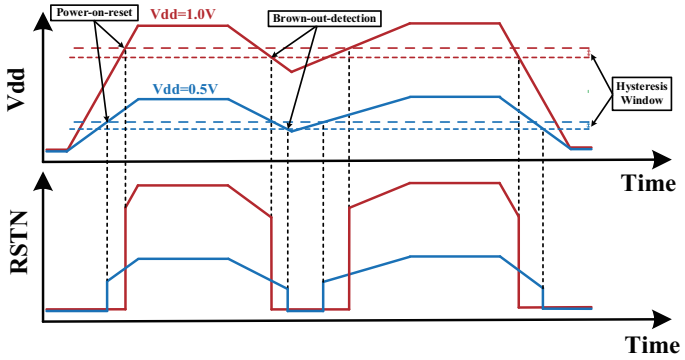

Fig 1 *Functional diagram of a POR circuit detecting multi-supply voltages with BOR function.*

comparator scalable and V2 is determined by the comparison of I1 and I2. When the power supply starts to ramp up, the 3T VR and the Vdd-tracking VR generate V1 and V2 respectively, then, the current of I1 and I2 rises gradually. Since the 3T VR and the Vdd-tracking VR both work in sub-threshold region, the current of these transistors can be calculated as follows [7]:

$$I_D = I_Q S e^{\frac{V_{GS}-V_{th}}{\eta V_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right), \qquad I_Q = \mu C_{OX} (\eta - 1) V_T^2, \tag{1}$$

where μ represents electron mobility, C_{OX} is gate oxide capacitance, and η is subthreshold slope factor ($\eta = 1 + C_d/C_{OX}$, where C_d is depletion capacitance), S is transistor aspect ratio. $V_T = K_B T/q$ is the thermal voltage, where K_B is Boltzmann constant, and q is the electron charge. The factor $1 - e^{-\frac{V_{DS}}{V_T}}$ in (1) can be ignored since the error is negligible for $V_{DS} > 4V_T$. According to the previous analysis of

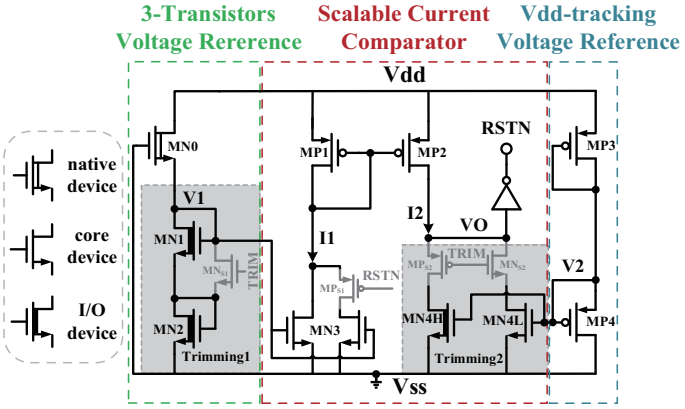

Fig 2 *Schematic circuit of the proposed reconfigurable POR circuit.*

ΔVth-based voltage references [7–9], by equating the current of MN0 and MN1/MN2, MP3 and MP4 respectively, we can obtain V1 and V2 as

$$V1 = M * [Vth_{n1} - \frac{\eta_{n1}}{\eta_{n0}} Vth_{n0} + \eta_{n1} V_T \ln \frac{S_{n0} I_{Q_{n0}}}{S_{n1} I_{Q_{n1}}}], \tag{2}$$

$$V2 = Vdd - (Vth_{p3} - \frac{\eta_{p3}}{\eta_{p4}} Vth_{p4} + \eta_{p3} V_T \ln \frac{S_{p3} I_{Q_{p3}}}{S_{p4} I_{Q_{p4}}}), \tag{3}$$

where parameter M represents the number of stacking self-biased NMOS transistors MN1 and MN2 in 3T VR. When the trimming signal TRIM is set to be low, parameter M is equal to 2 and V1 is large. When the trimming signal TRIM is set to be high, parameter M is equal to 1 and V1 is low. It can be seen from (2) and (3) that as Vdd continues to be powered on, V1 first remains stable while V2 continues to increase with Vdd. Then, I1 and I2 generated by MN3 and MN4 driven by V1 and V2 respectively are as follows

$$I1 = I_{Q_{n3}} N S_{n3} e^{\frac{V1 - V_{th_{n3}}}{\eta_{n3} V_T}}, \tag{4}$$

$$I2 = I_{Qn4} S_{n4} e^{\frac{V2 - Vth_{n4}}{\eta_{n4} V_T}}, \quad (5)$$

where parameter N represents the number of the optional current reference generator MN3. When the reset signal RSTN is low, parameter N is equal to 2. When the reset signal RSTN is high, parameter N is equal to 1. We assume that the current mirror is ideal, and when the Vdd-tracking current I2 increases equal to the current reference I1, with (4) and (5), the supply voltage as well as the trip-voltage of the POR circuit is as follow

$$V_{trip} = \frac{\eta_{n4}}{\eta_{n3}} V1 + Vth_{n4} - \frac{\eta_{n4}}{\eta_{n3}} Vth_{n3} + Vth_{p3} - \frac{\eta_{p3}}{\eta_{p4}} Vth_{p4} + V_T \left(\eta_{n4} \ln \frac{N S_{n3} I_{Q_{n3}}}{S_{n4} I_{Q_{n4}}} + \eta_{p3} \ln \frac{S_{p3} I_{Q_{p3}}}{S_{p4} I_{Q_{p4}}}\right), \quad (6)$$

It can be seen from (2) and (6) that the trip-voltage of the POR circuit is directly determined by the threshold voltages Vth and sizes of three pairs of transistors (MN0 and MN1/MN2, MN3 and MN4, MP3 and MP4), the trimming signal TRIM and the reset signal RSTN. The trimming signal TRIM can be set in advance by digital circuit according to the system mode. When TRIM = 1, the switch transistor MNS1 is off and the lower V1 is used to generate the lower current reference I1. Meanwhile, since the switch transistor MNS2 is on while the switch transistor MPS2 is off, the lower Vth core device MN4L is used to generate the lower Vdd-tracking current I2. Hence, the lower trip-voltage is generated to detect the lower supply power. When TRIM = 0, the switch transistor MNS1 is off and the higher V1 is used to generate the higher current reference I1. Meanwhile, since the switch transistor MNS2 is off while the switch transistor MPS2 is on, the higher Vth I/O device MN4H is used to generate the higher Vdd-tracking current I2. Hence, the higher trip-voltage is generated to detect the higher supply power. In addition, when the supply power is low, RSTN = 0 and MPS1 is on, from (4) the current reference I1 is larger so that the larger trip-voltage is generated as the POR trip-voltage (VPOR). And once the supply power becomes high, RSTN = 1 and MPS1 is off, from (4) the current reference I1 is lower so that the lower trip-voltage is generated as the BOD trip-voltage (VBOD). Thus, a hysteresis window is obtained due to the difference between VPOR and VBOD. According to above analysis, the proposed POR circuit can realize the detection of different voltages with BOD function.

One of the advantages of such ΔVth-based VRs like the 3T VR and the Vdd-tracking VR is to achieve temperature insensitivity by adjusting sizes of transistors [7–9]. Since the threshold voltage Vth is complementary to temperature [8] and V_T is proportional to temperature, the temperature coefficients (TC) of V1 and V2 in (2) and (3) can be canceled out, namely $dV1/dT = 0$ and $dV2/dT = 0$, by adjusting the sizes of MN0 and MN1/MN2, MP3 and MP4, respectively. For (6), TC of the trip-voltage can be expressed as

$$\frac{dV_{trip}}{dT} = \alpha_{n4} - \frac{\eta_{n4}}{\eta_{n3}} \alpha_{n3} + \frac{\eta_{n4} K_B}{q} \ln \frac{N S_{n3} I_{Q_{n3}}}{S_{n4} I_{Q_{n4}}} + \frac{\eta_{n4}}{\eta_{n3}} \frac{dV1}{dT} - \frac{dV2}{dT}, \quad (7)$$

where α is the first-order TC with a negative value. To simplify the analysis, the first-order temperature dependency of Vth and V_T is considered while the temperature dependency of μ and η as well as the second-order temperature dependency of Vth can be ignored. Similarly, by optimizing sizes of transistors MN3 and MN4 further, $dV_{trip}/dT = 0$ can be also achieved. Hence, a temperature-insensitivity POR circuit can be obtained. On the other hand, it can be observed from (6) that the Vth variation will affect the offset of the trip-voltage V_{trip}. Since there is another advantage of the ΔVth-based VRs that the Vth all appearing in pairs can cancel each other effect out by difference [8], as well as in the trip-voltage of the proposed POR circuit, three pairs of transistors in (6) significantly improves the robustness to process variations.

Simulation results: The performance of the proposed POR circuit has been determined in 55 nm CMOS process. Figure 3 shows the layout of the proposed POR circuit. With the all-MOS structure, the active area of the POR circuit is just 240 μm^2.

Figure 4 shows the transient waveforms of the proposed reconfigurable POR circuit for different supply voltage. When the proposed POR circuit is going to detect low supply and TRIM is set to be high, Figure 4(a) shows that the VPOR is 385.5 mV and the VBOD is 377.1 mV at room temperature and Vdd = 500 mV. In this case, the quiescent current of the proposed POR circuit is only 8.5 nA when RSTN is released. When the proposed POR circuit is going to detect high supply and TRIM is set to be low, Figure 4(b), the VPOR is 775.4 mV and the VBOD is 740.5 mV at room temperature and Vdd = 1 V. In this case, the quiescent current of the proposed POR circuit increases up to 92.6 nA when RSTN is released.

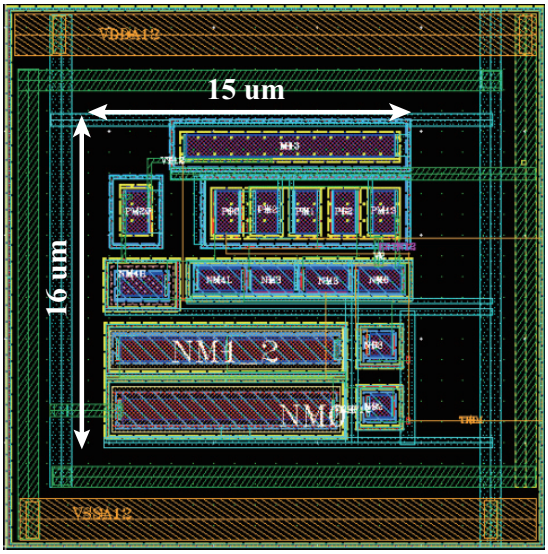

Fig 3 *Layout of the proposed POR circuit.*

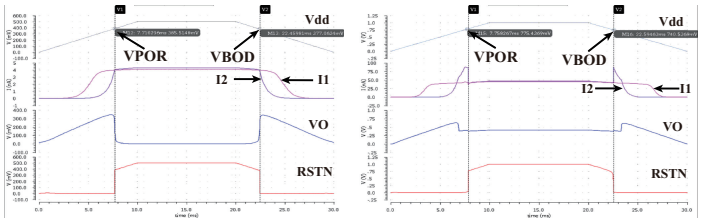

Fig 4 *Transient waveforms of the proposed POR circuit at (a) Vdd = 0.5 V; (b) Vdd = 1 V.*

Figure 5 shows the simulated temperature coefficients of the proposed reconfigurable POR circuit at Vdd = 0.5 V and Vdd = 1 V for the -40 °C to 125 °C temperature range. As Figure 5(a) shows, when Vdd = 0.5 V, the typical TC of VPOR is 168 ppm/°C and the average TC of different process corners of VPOR is 175.7 ppm/°C, meanwhile, the typical TC of VBOD is 185 ppm/°C and the average TC of different process corners of VBOD is 172.3 ppm/°C. As Figure 5(b) shows, when Vdd = 1 V, the typical TC of VPOR is 441 ppm/°C and the average TC of different process corners of VPOR is 412.3 ppm/°C, meanwhile, the typical TC of VBOD is 351 ppm/°C and the average TC of different process corners of VBOD is 380.3 ppm/°C. The differences between the average TC and the TC at different process corners above are not large, which indicates that the proposed circuit can achieve temperature insensitivity well with process deviations.

In order to test the performance impacted by CMOS process, Monte Carlo simulations are required. Figure 6 shows 1000 points Monte-Carlo simulation results of the proposed POR circuit at different supply voltage considering both global variation and local mismatch. At the temperature of 25 °C and Vdd = 0.5 V, the mean VPOR is 386 mV with a standard deviation of 8.1 mV and the mean VBOD is 377.4 mV with a standard deviation of 6.6 mV. When Vdd = 1 V, the mean VPOR is 772.3 mV with a standard deviation of 11.2 mV and the mean VBOD is 738.1 mV with a standard deviation of 9.7 mV.

Table 1 summarises the performance of the proposed reconfigurable POR circuit in comparison with state-of-the-art POR designs. It can be noted that with a flexible power management strategy, the proposed POR

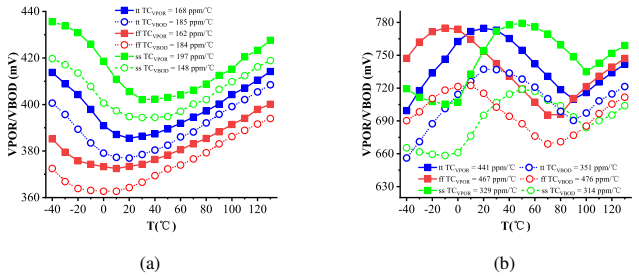

Fig 5 *PVT simulation results of temperature coefficients at (a) Vdd = 0.5 V; (b) Vdd = 1 V.*

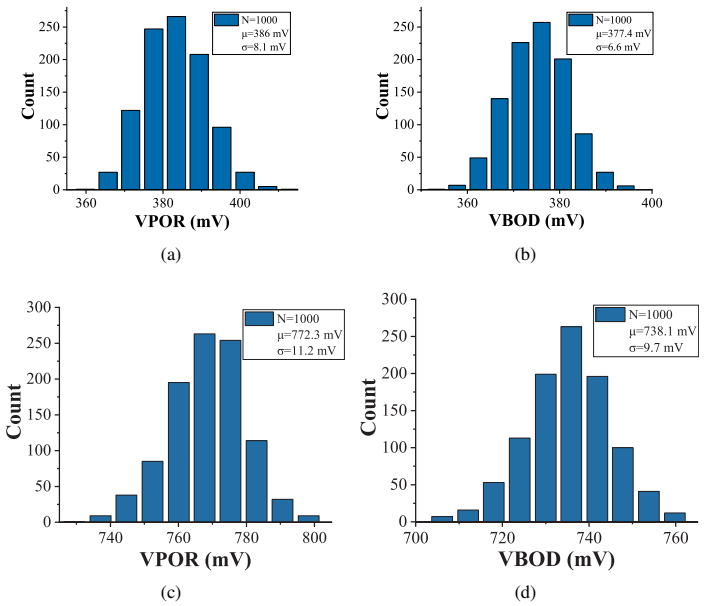

Fig 6 *Monte-Carlo simulation results of the proposed POR circuit (a) VPOR at Vdd = 0.5 V; (b) VBOD at Vdd = 0.5 V; (c) VPOR at Vdd = 1 V; (d) VBOD at Vdd = 1 V.*

Table 1. Comparison with Various POR designs

Parameter	This work	[2]	[5]	[6]
Process (nm)	55	65	180	65
Type	Current	Bandgap	Delay	Bandgap
Supply voltage (V)	0.5 to 1	1	1.8 to 3.3	0.65
POR Trip Voltage (mV)	385.5/757.4	840	1.33/1.63/2.11	0.59
Multi-Level	Yes	No	Yes	No
Brown-out detection	Yes	Yes	No	No
Quiescent current (nA)	8.5/92.6	5000	19.17	4000
Temp. range (°C)	-40 to 125	N.A	-40 to 125	-10 to 110
TC (ppm/°C)	168/441	N.A.	N.A.	292
Area (μm^2)	240	N.A.	5700	950
Results	Sim.	Sim.	Sim.	Meas.

circuit shows the lowest quiescent current and temperature insensitivity compared with other POR circuits. The configurable trip voltage makes the proposed POR circuit very suitable for MSV systems. Moreover, with the resistor-less structure, the proposed POR circuit shows better area efficiency.

Conclusion: In this letter, an ultra-low-power power-on-reset circuit with reconfigurable trip-voltages is proposed. With the threshold difference voltage references and scalable current comparator, all-MOS subthreshold architecture is realised to reduce area and power consumption overhead. Simulation results based on 55 nm CMOS process show that the proposed power-on-reset circuit generates trip voltages of 385.5 mV and 775.4 mV, consuming only 8.5 nA and 92.6 nA at the supply voltage of 0.5 V and 1 V, respectively. The typical temperature coefficients of trip-voltages for the supply of 0.5 V and 1 V is 168 ppm/°C and 441 ppm/°C. And the area of the proposed power-on-reset circuit is as low as 240 μm^2. Overall, the proposed POR circuit has accurate trip-voltage, low static power, and small area, which is very suitable for low-power and multi-supply systems.

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